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Main V1495 module in DS-50 Global trigger mode

(Firmware release 6)

This document describes Main V1495 trigger logic firmware for the DS-50 global trigger scheme. The Main V1495 module communicates with the Veto V1495 module located in the control room. When a trigger is generated at the module output along with the Trigger ID, the Trigger ID is serially encoded and sent via Port F output to the Veto V1495 module. The Main V1495 module receives Veto trigger inhibit signal from the Veto V1495 module. The Main V1495 also receives Veto trigger request signals and processes them along with other trigger sources. There are two processing modes for the Veto trigger requests: TPC only and Pass through. In the TPC only mode Veto triggers are sent to the Veto DAQ only during ADC data acquisition window set by internal register. In the Pass through mode Veto triggers are also sent to the Veto DAQ when the TPC DAQ system is not busy. The main purpose of the firmware is to generate trigger signal for the TPC ADCs and Veto DAQ. There are several sources of the trigger requests that could generate a trigger. All trigger requests are processed by the Main V1495 module and synchronized with the high accuracy external 50 MHz clock^[1]. Main trigger request sources are Majority Trigger Logic and two Veto trigger requests. Two signals at Port E provide External trigger and External Laser trigger requests. There are also two internal programmable fixed frequency generators and one internal random frequency generator. The module could also be used as a trigger pattern source to simulate TPC trigger pattern on 16-bit wide test port. The Main V1495 module also generates delayed TDC triggers for the CAEN V1190 TDCs running in a common stop mode. A PLL generated 40 MHz ECL clock signal is provided as required by the TDC spec. A block-diagram of the firmware logic is presented in Figure 1.

The firmware uses existing VME interface designed by CAEN and implemented in the VME FPGA. The VME interface firmware cannot be modified by the user. The DS-50 trigger logic is implemented in the User FPGA and is fully modifiable except for the pins assignment. The firmware contains 32x4K FIFO memory, which is used as a temporarily storage for the event data (Event FIFO). The FIFO memory has to be read out after a trigger is generated by the module. A VME interrupt is generated when the FIFO memory becomes not empty. The depth of the FIFO is set by a programmable register and has to match the number of buffers in the ADCs. If the FIFO becomes full, all triggers are disabled until at least one event is read out from it. The triggers are also disabled when any of the ADCs become busy. This is provided by using chained OR at the ADC I/O port. Two Port E inputs are used to accept ADC busy signals. Additional inhibit time can be added after ADC busy signal goes low (becomes inactive) by enabling Memory Full extension. This programmable one-shot will trigger on falling edge of the busy signal and extend trigger inhibit by a preset value. The Veto trigger inhibit signal (Veto MF) also disables all triggers. The Veto V1495 module has identical logic for extending Veto DAQ Memory Full signal.

The Memory Full Logic (MF Logic) can be run in two modes: LNGS and FNAL. In FNAL mode some of the Port F outputs are switched to different signal sources. LNGS mode is the default mode of

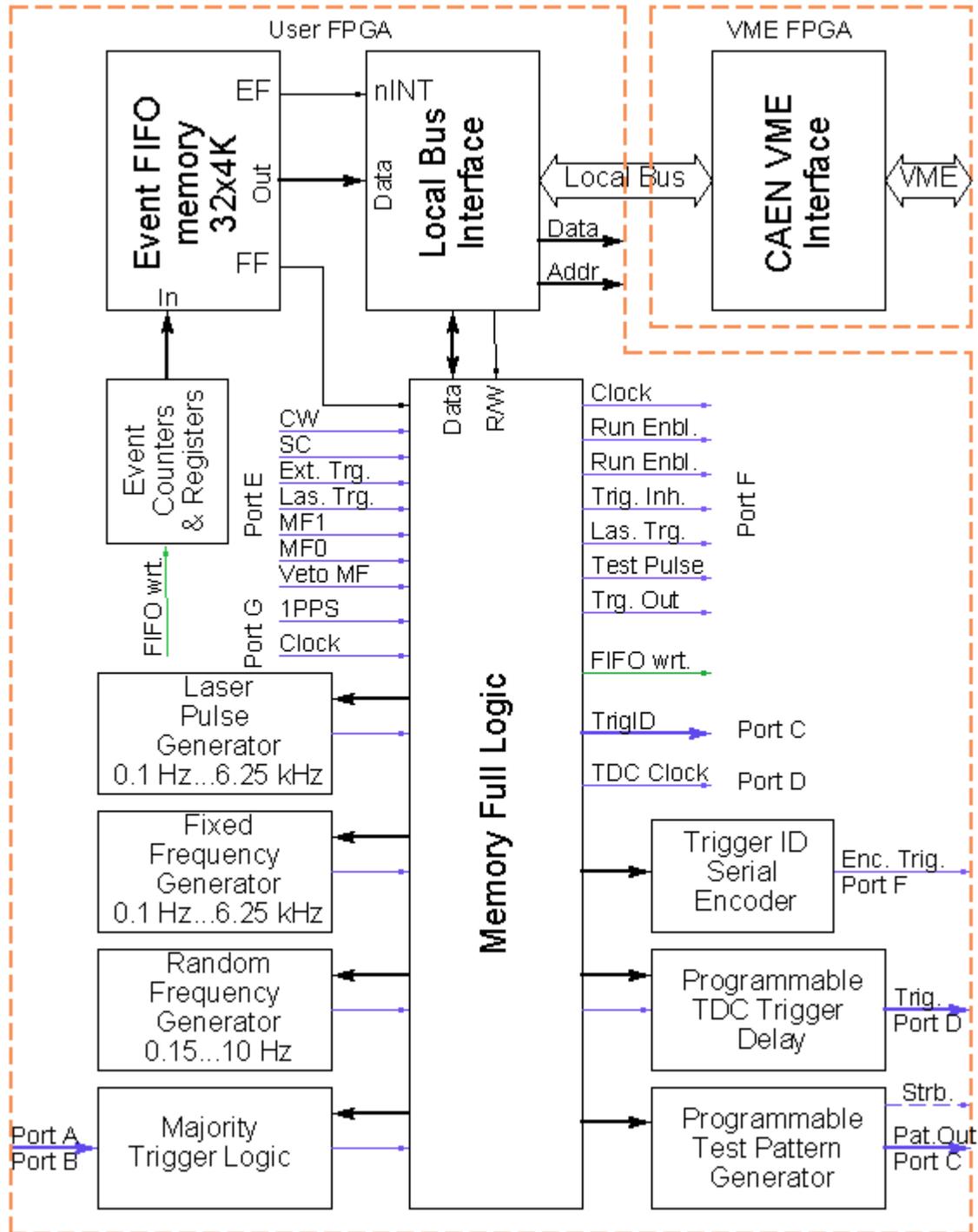


Figure 1. Main V1495 firmware logic.

operation. The MF Logic can also be run in a pass-through mode when every trigger request signal will be sent to the output. Any trigger source can be enabled or disabled using Trigger Control register. The MF logic generates two copies of the 8-bit Trigger number signal that are hooked up to two ADCs in the TPC crate. Also, the 16-bit value of the Trigger ID is serially encoded^[2] and sent to the Veto V1495. This value of the Trigger ID embedded in the ADC event header is used for event synchronization. A full 12-bit value of the Trigger number and current trigger type are stored in the Event FIFO memory. The firmware also provides various counters running off 1PPS and 50 MHz clock signals. This feature provides additional timing synchronization information for the event.

When V1495 module generates a trigger, any consequent trigger requests are blocked by the MF logic to avoid sending triggers to the TPC ADC modules while they are digitizing current event. This prevents a loss of the event synchronization between V1495 and ADCs, and is facilitated by a programmable one-shot and a signal from the Event FIFO write state machine. The duration of the one-shot pulse is selected by the value of the ADC Data Acquisition Window Inhibit register described below. It should exceed actual ADC acquisition window by a few uS. At the end of the one-shot pulse timing counters values and data of the various registers are stored in the Event FIFO. Trigger requests are

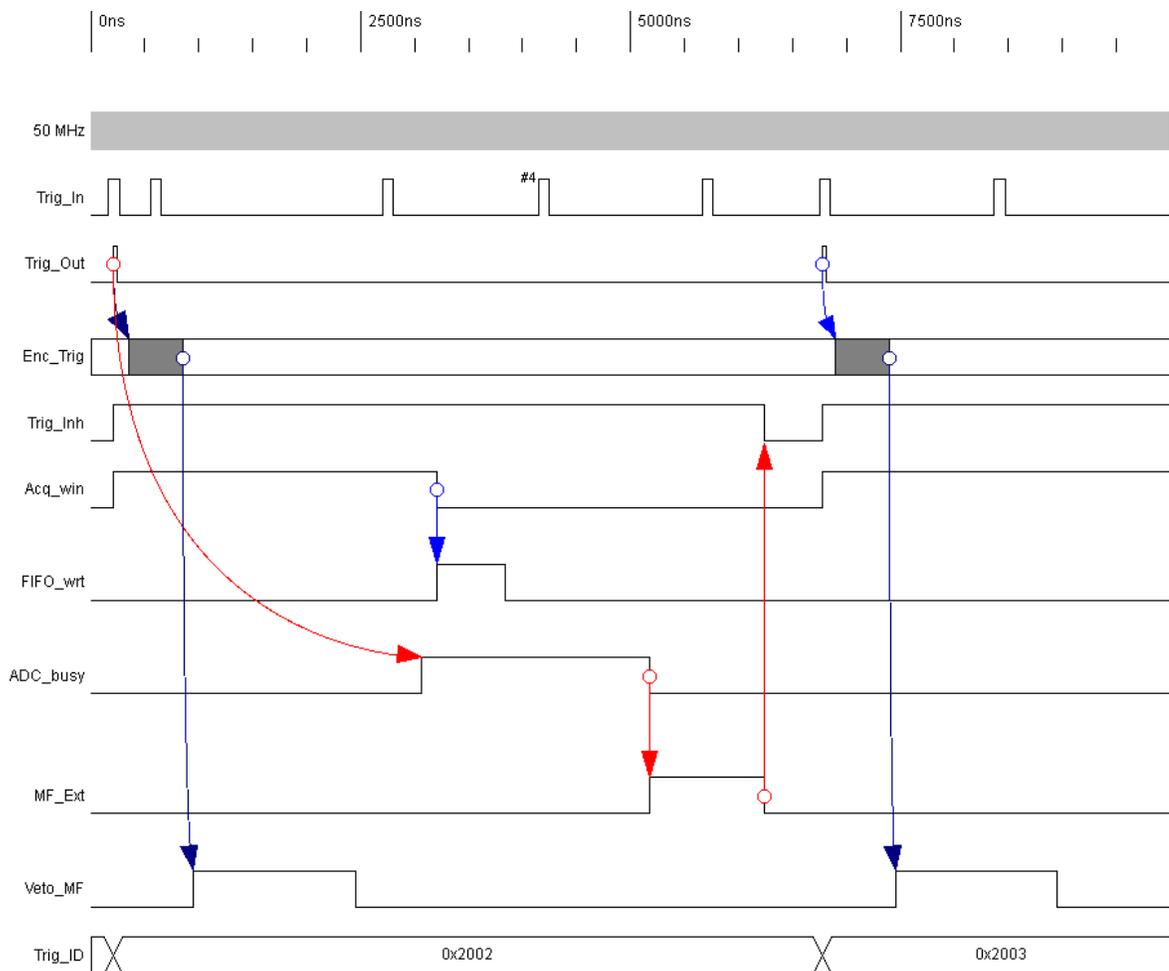


Figure 2. V1495 timing diagram.

disabled while data is written to the Event FIFO as well. After writing data is finished, a new trigger request can be accepted. Any busy signal from the TPC ADCs or Veto MF signal could also block trigger requests, if present at the time when the MF logic opens for the next trigger. At the end of the ADC busy signal an MF extension one-shot may be fired, if it is enabled. This will extend the duration of the ADC busy Inhibit for additional time set by the MF Extension Inhibit register. This was found necessary for the earlier version of the CAEN V1720 ADC firmware^[3], but may not be needed for the current version. The timing diagram (not to scale) illustrating described functionality is shown in Figure 2 above. As shown in the figure, there is only one buffer available in the ADCs, therefore, ADC busy signal is generated when event data is transferred to the ADC output buffer. If there were no ADC busy signal, the next trigger request labeled #4 would be accepted.

The default base address of the V1495 module is 0x01000000. The upper 16 bits of the address are set by four rotary switches at the far end of the board. The front panel User LED has the following functions:

- Red – no clock signal at G0 input
- Flashing green – trigger generated by the module

Firmware type register

Address: Base + 0x100C
 Size: 32 bit
 Mode: R

Bit	Function	Default
[3:0]	Firmware release	6
[7:4]	V1495 module type	1
[31:8]	N/A	0x000000

Note: The Main V1495 module type is 1.

Port A mask register

Address: Base + 0x1010
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[31:0]	Port A mask bits, 1 - enable	0xFFFFFFFF

Note: Port A inputs [30:16] and [14:0] are used in the TPC trigger logic.

Port B mask register

Address: Base + 0x1014
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[31:0]	Port B mask bits, 1 - enable	0xFFFFFFFF

Note: Port B inputs [9:0] are used in the TPC trigger logic.

Run Control register

Address: Base + 0x1018

Size: 32 bit

Mode: R/W

Bit	Function	Default
[0]	Run Enable, 1 - enable	0
[1]	Memory Full Inhibit enable, 1 - enable	0
[2]	Extension of the MF signal enable , 1 - enable	0
[3]	Veto Memory Full Inhibit enable, 1 - enable	0
[4]	Pause run, 1 - pause	0
[14:5]	Reserved	b0000001000
[15]	FNAL mode, 1 - enable	0
[31:16]	Internal Test pulser frequency 0.1 Hz – 6.25 kHz	0x0000

Note: Writing 0x3 or 0x7 to this register starts the run, writing 0x0 stops the run.

Bit [4] can be used for disabling triggers. All triggers are disabled when this bit is set to 1.

Any combination of bits [31:16] can be used to set trigger frequency. Value 0xFFFF corresponds to ~ 0.1 Hz frequency; value 0x0000 corresponds to ~ 6.25 kHz frequency. In FNAL mode two trigger signals and Pattern strobe signal are applied to ports F0, F2 and F3 respectively.

ADC Data Acquisition Window Inhibit register

Address: Base + 0x101C

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	ADC data acquisition window, 20 ns step	0x00003C8C

Note: This setting must exceed the actual ADC data acquisition window width by a few microseconds.

MF Extension Inhibit register

Address: Base + 0x1020

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	MF Extension pulse duration, 20 ns step	0x000009C4

Note: This setting is used to add additional time to trigger inhibit after Memory Full signal transitions to zero. If Almost Full register setting of the ADC is not equal to zero, this functionality can be disabled by using value 0x3 to start the run.

Trigger Control register

Address: Base + 0x1024
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[0]	TPC trigger enable, 1 - enable	1
[1]	Internal fixed frequency trigger enable, 1 - enable	0
[2]	Internal random frequency trigger enable, 1 - enable	0
[3]	Reserved	0
[4]	Veto CW trigger enable, 1 - enable	0
[5]	Veto SC trigger enable, 1 - enable	0
[6]	Reserved	0
[7]	Reserved	0
[8]	Laser trigger enable, 1 - enable	0
[9]	External trigger enable, 1 - enable	1
[10]	Test Pattern Pulser enable, 1 - enable	0
[11]	Reserved	0
[12]	Pass through Veto triggers enable, 1 - enable	0
[15:13]	Reserved	0x0
[19:16]	Majority logic Time Window, 10 ns step	5
[25:20]	Majority logic Low Threshold	5
[31:26]	Majority logic High Threshold	39

Note: Bits [15:0] are Trigger mask bits, bits [31:16] control TPC majority trigger logic. Frequency range of the internal random pulser is 0.15 Hz - 10 Hz. If Pass through bit is set to enable, Veto triggers are sent directly to the Veto V1495 module anytime they are accepted by the Main V1495 module; otherwise they are only sent during ADC data acquisition window (see register 0x101C above).

Run Number register

Address: Base + 0x1028
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[31:0]	Run Number	0x00001111

Test Pulser DPM write register

Address: Base + 0x102C
 Size: 32 bit

Mode: R/W

Bit	Function	Default
[0]	Time/Pattern select, 1 - Time	0
[1]	Address/Data select, 1 - Address	0
[2]	Reserved	0
[3]	Reserved	0
[4]	Read/Write select, 1 - Read	0
[5]	Reserved	0
[6]	Reserved	0
[7]	Single Sequence/Free Run select, 1 - Single Sequence	0
[15:8]	Reserved	0x00
[31:16]	DPM Write Data	0x0000

Status register

Address: Base + 0x1030
 Size: 32 bit
 Mode: R

Bit	Function	Default
[0]	FIFO read empty flag, 1 - empty	1
[1]	FIFO write full flag, 1 - full	0
[2]	FIFO write empty flag, 1 - empty	1
[3]	FIFO read full flag, 1 - full	0
[4]	Trigger request status, 1 - pending	0
[5]	Simulated FIFO Empty flag, 1 - empty	1
[6]	Simulated FIFO Full flag, 1 - full	0
[7]	FIFO state machine error, 1 - error	0
[8]	Trigger inhibit signal, 1 - active	0
[14:9]	Reserved	0
[15]	PLL locked, 1 - locked	0
[27:16]	Trigger number	0x000
[31:28]	Trigger type	0x0

Note: The Trigger number is incremented with every trigger generated by the Main V1495 logic (see trigger types table below). The Simulated FIFO Empty flag is set to one when the number of generated triggers matches the number of processed interrupt requests. The Simulated FIFO Full flag is set to one when there are 16 (default value of the Event FIFO depth register) or more triggers awaiting readout. First event stored in the FIFO has Simulated FIFO Empty flag equal to one.

Test Pulser DPM read register

Address: Base + 0x1034
 Size: 32 bit

Mode: R

Bit	Function	Default
[15:0]	N/A	0x0000
[31:16]	DPM Read Data	0x0000

TDC Reference Trigger delay register

Address: Base + 0x1044

Size: 32 bit

Mode: R/W

Bit	Function	Default
[23:0]	TDC trigger output delay, 20 ns step	0x4C4B40
[31:24]	N/A	0x00

Note: This setting is used to delay V1495 TDC trigger outputs at Port D for a fixed amount of time. The width of the ADC Data Acquisition Window must exceed this delay value otherwise some TDC reference triggers will be lost.

Laser Trigger control register

Address: Base + 0x1048

Size: 32 bit

Mode: R/W

Bit	Function	Default
[0]	Enable internal pulser, 1 - enable	0
[1]	Enable Port E5 laser trigger input, 1 - enable	0
[15:2]	N/A	0x0000
[31:16]	Laser pulser frequency 0.1 Hz – 6.25 kHz	0x0000

Note: Bits [0:1] allow using external and internal signal sources in any combination. Bits [31:16] setting selects laser trigger frequency in the range 0.1 Hz – 6.25 kHz. Any combination of bits [31:16] can be used to set the frequency. Value 0xFFFF corresponds to ~ 0.1 Hz frequency; value 0x0000 corresponds to ~ 6.25 kHz frequency.

Event FIFO depth register

Address: Base + 0x104C

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	Event FIFO depth threshold, max 0x4C (75), default 16	0x10
[31:8]	N/A	0x000000

Note: The value of this register must not exceed the number of event buffers in the ADC setting.

Module ID/scratch register

Address: Base + 0x1050

Size: 32 bit

Mode: R/W

Bit	Function	Default
[7:0]	Module ID value	0x17
[31:8]	Scratch register	0x000000

Note: This register sets Module ID value and can be used to store user data in bits [31:8].

Table 1. Main V1495 trigger types

Trigger type	Comment	Value (decimal)
Reserved	N/A	1
Laser trigger	Port E5 or fixed frequency trigger	2
External trigger	Generated by a signal at Port E4	3
Internal pulser	Internal fixed frequency trigger	4
Random pulser	Internal random frequency trigger	5
Reserved	N/A	6
TPC trigger	Generated by TPC majority logic	7
Reserved	Used in Veto V1495	8
Reserved	Used in Veto V1495	9
Reserved	Used in Veto V1495	10
Reserved	Used in Veto V1495	11
Global Veto CW trigger	Generated by a signal at Port E7	12
Global Veto SC trigger	Generated by a signal at Port E6	13
Pass through Veto CW trigger	Generated by a signal at Port E7	14
Pass through Veto SC trigger	Generated by a signal at Port E6	15

Reset IRQ latch register

Address: Base + 0x1080

Size: 32 bit

Mode: W

Bit	Function	Default
[31:0]	Write only	N/A

Note: Writing to this register resets pending trigger request. The request is set every time an event is written to the Event FIFO memory.

IRQ Level register

Address: Base + 0x8004
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[2:0]	IRQ level, 1 - 7	0
[31:3]	Reserved	N/A

Note: If the value of bits [2:0] is zero, interrupts are disabled. The selected IRQ level is active when Event FIFO memory is not empty.

IRQ Status ID register

Address: Base + 0x8006
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[15:0]	IRQ ID	0xDDDD
[31:16]	Reserved	N/A

Note: Sets the IRQ Status ID value. The V1495 accepts DO8 and D16 VME IACK cycles.

Module Reset register

Address: Base + 0x800A
 Size: 32 bit
 Mode: W

Bit	Function	Default
[31:0]	N/A	N/A

Note: Writing to this register resets V1495 to a default state.

Event FIFO memory data format

Shown below is a format of the FIFO event data written for each trigger. The FIFO memory can be read out at the address 0x2000 using single VME read commands. It also can be read using V2718 DMA feature and CAENVME_FIFOBLTReadCycle library call. In order to enable V2718 DMA mode set bit 10 of the Control register at the address 0x01 to one. The number of data bytes in one event is 52.

31	23	15	7	0
Run number		Firmware type	Data length (bytes)	
Status register		Trigger ID		
Majority Logic Setup register		Trigger mask register		

Module ID	GPS Coarse Time counter [23:0], (sec.)		
GPS Fine Time counter [31:0], (20 ns)			
GPS One Second counter [31:0], (20 ns)			
TPC Trigger Pattern (TP) [31:0]			
0x000000			TPC TP [39:32]
Trigger counter [31:0]			
SC triggers received	CW triggers received	SC triggers sent	CW triggers sent
Total trigger inhibit time (x1 μ S)			
Trigger inhibit time for the previous trigger (x100 ns)			
Live time for the current trigger (x100 ns)			

Note: Firmware type is an 8-bit value, which includes firmware revision bits [11:8] and V1495 board type bits [15:12]. Sent Veto trigger counters represent the number of accepted Veto DAQ CW and SC triggers. Received Veto trigger counters represent total number of CW and SC triggers received during V1495 data acquisition window.

Note that GPS Time counters are implemented in the following way. The 24-bit GPS Coarse Time counter (counting 1PPS pulses) is reset by a VME reset or rising edge of the Run Enable signal (start of the run). The 32-bit GPS Fine Time counter (counting 50 MHz clock pulses) is reset by a VME reset or rising edge of the Run Enable signal (start of the run) or 1PPS signal. The 32-bit GPS One Second counter (counting 50 MHz clock pulses) is reset by a VME reset or rising edge of the Run Enable signal (start of the run). The GPS Coarse Time and GPS Fine Time counters are latched for each event by the V1495 trigger output and stored in the Event FIFO. The GPS One Second counter is latched by the 1PPS pulse and stored in the Event FIFO.

The TPC Trigger Pattern (TP) register works differently for different types of triggers. If Laser trigger is disabled, TP register stores trigger bit pattern for every trigger request accepted from the TPC Majority Logic. If Laser trigger bit and any of two Laser triggers are enabled, the TP register stores trigger bit pattern generated by the TPC Majority logic within ~500 ns gate after the trigger output is generated. The register also is reset at the beginning of the 500 ns gate.

The last three counters in the Event FIFO memory implemented for DS-50 live time corrections. All counters are 32-bit long, and could reach their maximum value. Per-trigger counters (Trigger inhibit time for the previous trigger and Live time for the current trigger) reach it at ~429 seconds. Total dead time counter rolls over at ~72 minutes. Per-trigger counters count 10 MHz clock, Total dead time counter counts 1 MHz clock. Per-trigger counters stop when they reach maximum value of 0xFFFFFFFF and retain it until next reset. They are reset by the V1495 trigger output. All counters are also reset at the rising edge of the Run Enable signal. All counters use the same total trigger inhibit signal as clock enable or disable. This signal is also available at port F4 of both V1495 for independent checks.

Port designations for the current version of the V1495 firmware (V1495 Main, v3):

- Port A [14..0] - LVDS, TPC trigger inputs
- Port A [30..16] - LVDS, TPC trigger inputs
- Port B [9..0] - LVDS, TPC trigger inputs

- Port C [7..0] - LVDS, Trigger Ordinal (8 bit) output
- Port C [15..8] - LVDS, Trigger Ordinal (8 bit) output
- Port C [31..16] - LVDS, Test pattern (16 bit) output
- Port D [0..2] - ECL, TDC clock signals (3 copies) - 40 MHz (PLL generated) outputs
- Port D [5..12] - ECL, V1495 trigger outputs (8 copies)
- Port E7 - TTL, Veto CW trigger input
- Port E6 - TTL, Veto SC trigger input
- Port E5 - TTL, External Laser trigger input
- Port E4 - TTL, External trigger input
- Port E3 - TTL, Memory Full OR from ADCs input
- Port E2 - TTL, Memory Full OR from ADCs input
- Port E1 - TTL, Veto Memory Full input
- Port F7 - TTL, External clock output
- Port F6 - TTL, Run Enable output
- Port F5 - TTL, Run Enable output
- Port F4 - TTL, Trigger inhibit signal
- Port F3 - TTL, Laser trigger output (default) OR Pattern strobe (FNAL mode)
- Port F2 - TTL, Test pulse output (default) OR V1495 trigger output (FNAL mode)
- Port F1 - TTL, V1495 trigger output
- Port F0 - TTL, Encoded trigger output (default) OR V1495 trigger output (FNAL mode)
- Port G0 - TTL, External clock input
- Port G1 - TTL, 1PPS signal input

References

- [1] B.Baldin, "DS50 Clock Fanout Module", November 2012, DarkSide document database: [DarkSide-doc-471-v2](#).
- [2] B.Baldin, S.Hansen, "DS-50 serial Trigger ID protocol", October 2013, DarkSide document database: [DarkSide-doc-713-v1](#).
- [3] B.Baldin *et al.*, "Study of the Memory Full signals of CAEN V1720 ADCs", October 2012, DarkSide document database: [DarkSide-doc-460-v4](#).