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DS-50 serial Trigger ID protocol

Electrical definition:

The signal level is TTL terminated with 50 ohms. The encoding scheme is FM with bits represented as two frequencies: 50 MHz (logic 1) and 25 MHz (logic 0) (see Fig. 1). Receiver is required to phase lock to the system clock (50 MHz). Data transmitted by the Trigger module will be at a known frequency, and a fixed but unknown phase with respect to the clock.

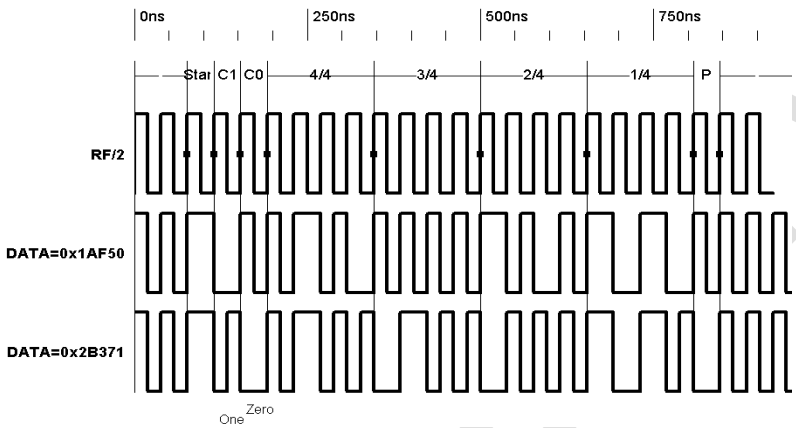

Figure 1 FM Encoding

Logical definition:

The information is transmitted serially as packets called frames. Each frame consists of a 20 bit sequence beginning with a start bit (S=0) followed by 18 bits of data, and a parity bit (P) (see Fig. 2).

Bit Position																		
Start Bit	Cmd. Bits		Data Bits															Parity
S	**C1**	**C0**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**	**D07**	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**	**P**

Figure 2 Frame Definition

A minimum interval of at least one clock period between frames is required. A string of 1's is sent between frames. The first four bits of the data field are used to distinguish between different trigger types. Two control codes (C1, C0) are used to define begin event and end event frame (currently not used).

Trigger message format

Trigger message (Trigger ID) includes event synchronization data (E0…E11) and trigger type bits (T0…T3). At least a portion of the lower 12 data bits should be included in the ADC data header.

C1	C0	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	**0**	**T3**	**T2**	**T1**	**T0**	**E11**	**E10**	**E9**	**E8**	**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**	**E0**

Preliminary