

Veto V1495 module Registers

(Firmware release 3)

The Veto V1495 module is a part of the DS50 Global Trigger logic described elsewhere. Currently it has two modes of operation: Local and Global. In Local mode module accepts two external Veto trigger requests and generates local trigger ID that can be used by the Veto DAQ system. In Global mode module receives all trigger information from the Main V1495 module. In both cases module provides trigger and clock signals for the Veto DAQ system. Additional Fanout V1495 module has to be used to provide a copy of trigger, clock and Trigger ID signals for each of four Veto DAQ crates. Below is a description of the Veto V1495 trigger logic firmware registers. Some of the registers are used in Local mode only, while the others are active in both modes of operation (see notes for each register). The default base address of the Veto V1495 module is 0x02000000. The upper 16 bits of the address are set by four rotary switches at the far end of the board. The front panel User LED has the following functions:

- Red – no clock signal at G0 input
- Flashing green – trigger generated by the module

Firmware type register

Address: Base + 0x100C
Size: 32 bit
Mode: R

Bit	Function	Default
[3:0]	Firmware release	3
[7:4]	V1495 module type	2
[31:8]	N/A	0x0000000

Note: The Veto V1495 module type is 2.

Port A mask register

Address: Base + 0x1010
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	Port A mask bits, 1 - enable	0xFFFFFFFF

Note: Port A inputs [1:0] are used in the Veto trigger logic as SC and CW trigger inputs respectively.

Port B mask register

Address: Base + 0x1014
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	Port B mask bits, 1 - enable	0xFFFFFFFF

Note: Port B inputs B[16] and B[17] are used as TDC OUT_PROG signals.

Run Control register

Address: Base + 0x1018
Size: 32 bit
Mode: R/W

Bit	Function	Default
[0]	Run Enable, 1 - enable	0
[1]	Memory Full Inhibit enable, 1 - enable	0
[2]	Extension of the MF signal enable , 1 - enable	0
[3]	Reserved	0
[4]	Pause run, 1 - pause	0
[5]	Reserved	0
[6]	Reserved	0
[7]	Reserved	0
[15:8]	Reserved	0x02
[31:16]	Internal trigger frequency 0.1 Hz – 6.25 kHz	0x0000

Note: When the Local mode is disabled (see Veto Trigger Control Register), bits [4] and [0] have no effect. Writing 0x3 or 0x7 to this register starts the local run, writing 0x0 stops the run. Bit [4] can be used for disabling triggers. Triggers are disabled when this bit is set to 1.

In Global mode this register has to be set to 0x2 or 0x6. Any combination of bits [31:16] can be used to set trigger frequency. Value 0xFFFF corresponds to ~ 0.1 Hz frequency; value 0x0000 corresponds to ~ 6.25 kHz frequency.

ADC Data Acquisition Window Inhibit register

Address: Base + 0x101C
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	ADC data acquisition window, 20 ns step	0x0000BB8

Note: This setting must exceed the actual Veto ADC data acquisition window width by a few microseconds.

MF Extension Inhibit register

Address: Base + 0x1020

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	MF Extension pulse duration, 20 ns step	0x00000032

Note: This setting is used to add additional time to trigger inhibit after Veto Memory Full signal goes to zero. This functionality can be disabled by using value of 0x3 when starting local run or 0x2 in Global mode.

Veto Trigger Control register

Address: Base + 0x1024

Size: 32 bit

Mode: R/W

Bit	Function	Default
[0]	External trigger (at port E6) enable, 1 - enable	1
[1]	Internal fixed frequency trigger enable, 1 - enable	0
[2]	Reserved	0
[3]	Reserved	0
[4]	CW trigger enable, 1 - enable	1
[5]	SC trigger enable, 1 - enable	1
[6]	Reserved	0
[7]	Local mode enable, 1 - enable	1
[31:8]	Reserved	0x000000

Note: Bits [5:0] are Trigger mask bits; bits [31:8] are not used. The Trigger mask bit settings are valid in Local mode only.

Run Number register

Address: Base + 0x1028

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	Run Number	0x00001234

Note: Used only in Global mode (See Event FIFO memory data format).

TDC Reference Trigger delay register

Address: Base + 0x102C

Size: 32 bit

Mode: R/W

Bit	Function	Default
[23:0]	TDC trigger output delay, 20 ns step	0x4C4B40
[31:24]	N/A	0x00

Note: This setting is used to delay V1495 TDC trigger outputs at Port D for a fixed amount of time. It is valid in Global mode only. There is no TDC trigger output in Local mode.

Status register

Address: Base + 0x1030
Size: 32 bit
Mode: R

Bit	Function	Default
[0]	FIFO read empty flag, 1 - empty	1
[1]	FIFO write full flag, 1 - full	0
[2]	FIFO write empty flag, 1 - empty	1
[3]	FIFO read full flag, 1 - full	0
[4]	Trigger request status, 1 - pending	0
[5]	Simulated FIFO Empty flag, 1 - empty	1
[6]	Simulated FIFO Full flag, 1 - full	0
[7]	FIFO state machine error flag, 1 - error	0
[8]	Trigger inhibit signal, 1 - active	0
[11:9]	Reserved	b000
[12]	Veto DAQ Error flag, 1 - error	0
[13]	FM decoder error flag, 1 – message error	0
[14]	FM decoder done flag, 1 – message received	0
[15]	PLL locked, 1 - locked	0
[27:16]	Trigger number	0x000
[31:28]	Trigger type	0x0

Note: Trigger number is incremented with every trigger generated by the MF logic in Local mode (see Trigger type table below). In Global mode this register holds the value received from the Main V1495 module. The Simulated FIFO Empty flag is set to one when the number of generated triggers matches the number of processed interrupt requests. The Simulated FIFO Full flag is set to one when there are 16 (default value of the Event FIFO depth register) or more triggers awaiting readout. First event stored in the FIFO has Simulated FIFO Empty flag equal to one. FM decoder flags are valid for the current trigger only. They are reset every time an event is written to the Event FIFO memory.

Event FIFO depth register

Address: Base + 0x104C
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	Event FIFO depth threshold, max 0x4C (75), default 16	0x10
[31:8]	N/A	0x000000

Note: The value of this register must not exceed the number of event buffers in the ADC setting. The Event FIFO memory will be read out in Global mode only.

Module ID/scratch register

Address: Base + 0x1050
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[7:0]	Module ID value	0x28
[31:8]	Scratch register	0x000000

Note: This register sets Module ID value and can be used to store user data in bits [31:8].

Table 1. Veto V1495 Trigger types

Trigger type	Comment	Value (decimal)
Reserved	Used by Main V1495 Trigger logic	1
Reserved	Used by Main V1495 Trigger logic	2
Reserved	Used by Main V1495 Trigger logic	3
Reserved	Used by Main V1495 Trigger logic	4
Reserved	Used by Main V1495 Trigger logic	5
Reserved	Used by Main V1495 Trigger logic	6
Reserved	Used by Main V1495 Trigger logic	7
Local Veto SC trigger	Generated by Veto Hardware trigger	8
Local Veto CW trigger	Generated by Veto Hardware trigger	9
Local Veto internal trigger	Generated by V1495 Veto logic	10
Local Veto External trigger	Generated by a signal at Port E6 (Veto)	11
Reserved	Used by Main V1495 Trigger logic	12
Reserved	Used by Main V1495 Trigger logic	13
Reserved	Used by Main V1495 Trigger logic	14
Reserved	Used by Main V1495 Trigger logic	15

Reset IRQ latch register

Address: Base + 0x1080

Size: 32 bit
 Mode: W

Bit	Function	Default
[31:0]	Write only	N/A

Note: Writing to this register resets pending trigger request. The request is set every time an event is written to the FIFO in Global mode.

IRQ Level register

Address: Base + 0x8004
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[2:0]	IRQ level, 1 - 7	0
[31:3]	Reserved	N/A

Note: If the value of bits [2:0] is zero, interrupts are disabled. Not used in Local mode.

IRQ Status ID register

Address: Base + 0x8006
 Size: 32 bit
 Mode: R/W

Bit	Function	Default
[15:0]	IRQ ID	0xDDDD
[31:16]	Reserved	N/A

Note: Sets the IRQ Status ID value. The V1495 accepts DO8 and D16 IACK cycles. Not used in Local mode.

Module Reset register

Address: Base + 0x800A
 Size: 32 bit
 Mode: W

Bit	Function	Default
[31:0]	N/A	N/A

Note: Writing to this register resets V1495 to a default state.

Event FIFO memory data format

Shown below is a format of the FIFO event data written for each trigger in the Global mode. The FIFO can be read out using address 0x2000 in a single VME read command. It also can be read using

V2718 DMA feature and CAENVME_FIFOBLReadCycle library call. In order to enable V2718 DMA mode set bit 10 of the Control register at the address 0x01 to one. The event data length is 52 bytes.

31	23	15	7	0
Run number		Firmware type		Data length (bytes)
Status register		Trigger ID		
Veto Trigger Control register [31:16]		Veto Trigger Control register [15:0]		
Module ID	GPS Coarse Time counter [23:0], (sec.)			
GPS Fine Time counter [31:0], (20 ns)				
GPS One Second counter [31:0], (20 ns)				
Port A [31:0] latched by the trigger output				
Port B [31:0] latched by the trigger output				
Trigger counter [31:0]				
0x00	0x00	0x00	0x19	
Total trigger inhibit time (x1 μ S)				
Trigger inhibit time for the previous trigger (x100 ns)				
Live time for the current trigger (x100 ns)				

Note: Firmware type is an 8-bit value, which includes firmware revision bits [11:8] and V1495 board type bits [15:12].

Note that GPS Time counters are implemented in the following way. The 24-bit GPS Coarse Time counter (counting 1PPS pulses) is reset by a VME reset or rising edge of the Run Enable signal (start of the run). The 32-bit GPS Fine Time counter (counting 50 MHz clock pulses) is reset by a VME reset or rising edge of the Run Enable signal (start of the run) or 1PPS signal. The 32-bit GPS One Second counter (counting 50 MHz clock pulses) is reset by a VME reset or rising edge of the Run Enable signal (start of the run). The GPS Coarse Time and GPS Fine Time counters are latched for each event by the V1495 trigger output and stored in the Event FIFO. The GPS One Second counter is latched by the 1PPS pulse and stored in the Event FIFO.

Port designations for the *current version* of the V1495 firmware (V1495 Veto, v1):

- Port A [0] - LVDS, Veto CW trigger input
- Port A [1] - LVDS, Veto SC trigger input
- Port B [16] - ECL, TDC1 OUT_PROG signal input
- Port B [17] - ECL, TDC2 OUT_PROG signal input
- Port C [15..0] - LVDS, Trigger ID output
- Port C [16] - LVDS, Veto 50 MHz clock output
- Port C [17] - LVDS, Veto trigger output
- Port C [18] - LVDS, Veto Run Enable output
- Port C [19] - LVDS, Veto 1PPS output
- Port D [0..2] - ECL, TDC clock signals (3 copies) - 40 MHz (PLL generated) outputs
- Port D [5..12] - ECL, Delayed V1495 trigger outputs (8 copies)
- Port E7 - TTL, Encoded trigger input

- Port E6 - TTL, Veto external trigger input
- Port E5 - TTL, Veto Run Enable input
- Port E3 - TTL, Veto Memory Full input
- Port E2 - TTL, Veto DAQ Error input
- Port F7 - TTL, Veto clock output
- Port F6 - TTL, Run Enable output
- Port F5 - TTL, Veto MF signal output
- Port F4 - TTL, Trigger inhibit signal
- Port F3 - TTL, Veto trigger output
- Port F2 - TTL, CW trigger output
- Port F1 - TTL, SC trigger output
- Port F0 - TTL, Encoded trigger ID output
- Port G0 - TTL, External clock input
- Port G1 - TTL, 1PPS signal input