

Fanout V1495 module Registers

(Firmware release 3)

The Fanout V1495 module is a part of the DS50 Global Trigger logic described elsewhere. The module has two modes of operation: Local mode and Global mode. In Local mode module accepts two external Veto triggers and generates local trigger ID that can be used by the Veto DAQ system. In the Global mode module receives all trigger information from the Veto V1495 module. In both cases module provides trigger and timing signals for the Veto DAQ system. The module provides TTL trigger, clock, Run Enable and 1PPS signals; and LVDS Trigger ID signals for each of four Veto DAQ crates. Below is a description of the Fanout V1495 firmware registers. At power up, the module defaults to the Local mode. The default base address of the Fanout V1495 module is 0x03000000. The upper 16 bits of the address are set by four rotary switches at the far end of the board. The front panel User LED has the following functions:

- Red – no clock signal at G0 input
- Flashing green – trigger generated by the module

Firmware type register

Address: Base + 0x100C
Size: 32 bit
Mode: R

Bit	Function	Default
[3:0]	Firmware release	3
[7:4]	V1495 module type	3
[31:8]	N/A	0x0000000

Note: The Fanout V1495 module type is 3.

Port A mask register

Address: Base + 0x1010
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	Port A mask bits, 1 - enable	0xFFFFFFFF

Note: Port A inputs [15:0] used in the Fanout V1495 module firmware as Trigger ID input signals. Port A inputs [19..16] are used as 1PPS, Run Enable, trigger and clock input signals respectively.

Port B mask register

Address: Base + 0x1014

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	Port B mask bits, 1 - enable	0xFFFFFFFF

Note: Port B inputs [1..0] are used as SC and CW trigger inputs respectively when running in the Local mode.

Run Control register

Address: Base + 0x1018

Size: 32 bit

Mode: R/W

Bit	Function	Default
[0]	Run Enable, 1 - enable	0
[1]	Reserved	0
[2]	Reserved	0
[3]	External Run Enable in Local mode, 1 - enable	1
[4]	Reserved	0
[5]	Reserved	0
[6]	Reserved	0
[7]	Local mode, 1 - enable	1
[15:8]	Reserved	0x03
[31:16]	Reserved	0x0000

Note: When the Local mode is disabled, bit [0] has no effect. Writing 0x81 to this register starts local run, writing 0x80 stops the run. Bit [3] enables external Run Enable to pass through in the Local mode.

Veto triggers prescale register

Address: Base + 0x101C

Size: 32 bit

Mode: R/W

Bit	Function	Default
[11:0]	CW trigger prescale value (1...4095)	0x001
[15:12]	Reserved	0x0
[27:16]	SC trigger prescale value (1...4095)	0x001
[31:28]	Reserved	0x0

Note: Veto triggers (CW and SC) can be prescaled using this register. Used in Local mode only.

Status register

Address: Base + 0x1030
 Size: 32 bit
 Mode: R

Bit	Function	Default
[14..0]	Reserved	0
[15]	PLL locked, 1 - locked	0
[27:16]	Trigger number	0x000
[31:28]	Trigger type	0x0

Note: Trigger number is incremented with every trigger generated by the Fanout V1495 in the Local mode. The trigger number is reset by the rising edge of the Run Enable signal set by bit [0] of the Run Control register. See Fanout V1495 trigger types in the following table.

Table 1. Fanout V1495 Trigger types

Trigger type	Comment	Value (decimal)
Reserved	Used by Main V1495 Trigger logic	1
Reserved	Used by Main V1495 Trigger logic	2
Reserved	Used by Main V1495 Trigger logic	3
Reserved	Used by Main V1495 Trigger logic	4
Reserved	Used by Main V1495 Trigger logic	5
Reserved	Used by Main V1495 Trigger logic	6
Reserved	Used by Main V1495 Trigger logic	7
Local Veto SC trigger	Generated by Veto Hardware trigger	8
Local Veto CW trigger	Generated by Veto Hardware trigger	9
Reserved	Used by Veto V1495 Trigger logic	10
Reserved	Used by Veto V1495 Trigger logic	11
Reserved	Used by Main V1495 Trigger logic	12
Reserved	Used by Main V1495 Trigger logic	13
Reserved	Used by Main V1495 Trigger logic	14
Reserved	Used by Main V1495 Trigger logic	15

Module Reset register

Address: Base + 0x800A
 Size: 32 bit
 Mode: W

Bit	Function	Default
[31:0]	N/A	N/A

Note: Writing to this register resets V1495 to a default state.

Port designations for the current version of the V1495 firmware (V1495 Fanout, v3):

- Port A [15..0] - LVDS, Veto Trigger ID signal inputs
- Port A [16] - LVDS, Veto 50 MHz clock input
- Port A [17] - LVDS, Veto trigger input
- Port A [18] - LVDS, Veto Run Enable input
- Port A [19] - LVDS, Veto 1PPS input
- Port B [0] - LVDS CW trigger input
- Port B [1] - LVDS SC trigger input
- Port C [15..0] - LVDS, Trigger ID output
- Port C [31..16] - LVDS, Trigger ID output
- Port D [15..0] - LVDS, Trigger ID output
- Port D [31..16] - LVDS, Trigger ID output
- Port E7 - TTL 1PPS signal output
- Port E6 - TTL 1PPS signal output
- Port E5 - TTL 1PPS signal output
- Port E4 - TTL 1PPS signal output
- Port E3 - TTL Run Enable signal output
- Port E2 - TTL Run Enable signal output
- Port E1 - TTL Run Enable signal output
- Port E0 - TTL Run Enable signal output
- Port F7 - TTL, Veto clock output
- Port F6 - TTL, Veto clock output
- Port F5 - TTL, Veto clock output
- Port F4 - TTL, Veto clock output
- Port F3 - TTL, Veto trigger output
- Port F2 - TTL, Veto trigger output
- Port F1 - TTL, Veto trigger output
- Port F0 - TTL, Veto trigger output
- Port G0 - TTL, External clock input
- Port G1 - TTL, 1PPS signal input