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Updated

Main V1495 module Registers

Below is a description of the Main V1495 trigger logic firmware registers. The default base address of the V1495 module is 0x01000000. The upper 16 bits of the address are set by four rotary switches at the far end of the board. The front panel User LED has the following functions:

- Red – no clock signal at G0 input
- Flashing green – trigger generated by the module

Firmware type register

Address: Base + 0x100C
Size: 32 bit
Mode: R

Bit	Function	Default
[3:0]	Firmware release	1
[7:4]	V1495 module type	1
[31:8]	N/A	0x0000000

Note: The Main V1495 module type is 1.

Port A mask register

Address: Base + 0x1010
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	Port A mask bits, 1 - enable	0xFFFFFFFF

Note: Port A inputs [31:0] used in the TPC trigger logic.

Port B mask register

Address: Base + 0x1014
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	Port B mask bits, 1 - enable	0xFFFFFFFF

Note: Port B inputs [7:0] used in the TPC trigger logic.

Run Control register

Address: Base + 0x1018

Size: 32 bit

Mode: R/W

Bit	Function	Default
[0]	Run Enable, 1 - enable	0
[1]	Memory Full Inhibit enable, 1 - enable	0
[2]	Extension of the MF signal enable , 1 - enable	0
[3]	Reserved	0
[4]	Pause run, 1 - pause	0
[15:5]	Reserved	bx00000001000
[31:16]	Internal trigger frequency 1 Hz – 65 kHz, 0 - disable	0x0000

Note: Writing 0x3 or 0x7 to this register starts the run, writing 0x0 stops the run.
Bit [4] can be used for disabling triggers. The triggers are disabled when the bit is set to 1.
Bit [16] corresponds to ~ 1 Hz, bit [31] corresponds to ~ 65 kHz.
Only one bit of the frequency setting can be set at a time.
If none of the bits is set (all zero) the internal pulser is disabled.

ADC Data Acquisition Window Inhibit register

Address: Base + 0x101C

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	ADC data acquisition window, 20 ns step	0x00003C8C

Note: This setting must exceed the actual ADC data acquisition window by a few microseconds.

MF Extension Inhibit register

Address: Base + 0x1020

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	MF Extension pulse duration, 20 ns step	0x000009C4

Note: This setting is used to add additional time to trigger inhibit after Memory Full signal goes to zero.

Trigger Control register

Address: Base + 0x1024

Size: 32 bit

Mode: R/W

Bit	Function	Default

[0]	TPC trigger enable, 1 - enable	1
[1]	Internal trigger enable, 1 - enable	1
[2]	Reserved	0
[3]	Reserved	0
[4]	Veto CW trigger enable, 1 - enable	0
[5]	Veto SC trigger enable, 1 - enable	0
[6]	Reserved	0
[7]	Reserved	0
[8]	Laser trigger enable, 1 - enable	0
[9]	External trigger enable, 1 - enable	1
[10]	Test Pattern Pulser enable, 1 - enable	0
[11]	Reserved	0
[15:12]	Reserved	0x0
[19:16]	Majority logic Time Window, 10 ns step	5
[25:20]	Majority logic Low Threshold	5
[31:26]	Majority logic High Threshold	39

Note: Bits [15:0] are trigger mask bits, bits [31:16] control TPC majority trigger logic.

Run Number register

Address: Base + 0x1028

Size: 32 bit

Mode: R/W

Bit	Function	Default
[31:0]	Run Number	0x00001111

Test Pulser DPM write register

Address: Base + 0x102C

Size: 32 bit

Mode: R/W

Bit	Function	Default
[0]	Time/Pattern select, 1 - Time	0
[1]	Address/Data select, 1 - Address	0
[2]	Reserved	0
[3]	Reserved	0
[4]	Read/Write select, 1 - Read	0
[5]	Reserved	0
[6]	Reserved	0
[7]	Single Sequence/Free Run select, 1 - Single Sequence	0
[15:8]	Reserved	0x00
[31:16]	DPM Write Data	0x0000

Status register

Address: Base + 0x1030

Size: 32 bit

Mode: R

Bit	Function	Default
[0]	FIFO read empty flag, 1 - empty	1
[1]	FIFO write full flag, 1 - full	0
[2]	FIFO write empty flag, 1 - empty	1
[3]	FIFO read full flag, 1 - full	0
[4]	Interrupt request status, 1 - pending	0
[5]	Simulated FIFO Empty flag, 1 - empty	
[6]	Simulated FIFO Full flag, 1 - full	
[14:7]	Reserved	0
[15]	PLL locked, 1 - locked	0
[27:16]	Trigger number	0x000
[31:28]	Trigger type	0x0

Note: Trigger number is incremented with every trigger generated by MF logic. See trigger type table below (currently not implemented). Simulated FIFO Empty flag is set to one when there are no events in the FIFO. Simulated FIFO Full flag is set to one when there are 16 or more events in the FIFO. The first event stored in the FIFO has simulated FIFO Empty flag set to one.

Test Pulser DPM read register

Address: Base + 0x1034

Size: 32 bit

Mode: R

Bit	Function	Default
[15:0]	N/A	0x0000
[31:16]	DPM Read Data	0x0000

Trigger types

Trigger type	Comment	Value (decimal)
Reserved		1
Laser trigger		2
External trigger	Generated by a signal at Port E4	3
Reserved		4
Reserved		5
Reserved		6
Local TPC trigger	Generated by TPC majority logic	7

Local Veto SC trigger	Generated by Veto Hardware trigger	8
Local Veto CW trigger	Generated by Veto Hardware trigger	9
Reserved		10
Reserved		11
Reserved		12
Reserved		13
Reserved		14
Reserved		15

Reset IRQ latch register

Address: Base + 0x1080
Size: 32 bit
Mode: W

Bit	Function	Default
[31:0]	Write only	N/A

Note: Writing to this register resets interrupt latch. The interrupt latch is set every time an event is written to the FIFO.

IRQ Level register

Address: Base + 0x8004
Size: 32 bit
Mode: R/W

Bit	Function	Default
[2:0]	IRQ level, 1 - 7	0
[31:3]	Reserved	N/A

Note: If the value of bits [2:0] is zero, interrupts are disabled.

IRQ Status ID register

Address: Base + 0x8006
Size: 32 bit
Mode: R/W

Bit	Function	Default
[15:0]	IRQ ID	0xDDDD
[31:16]	Reserved	N/A

Note: Sets the IRQ Status ID value. The V1495 accepts DO8 and D16 IACK cycles.

Module Reset register

Address: Base + 0x800A

Size: 32 bit

Mode: W

Bit	Function	Default
[31:0]	N/A	N/A

Note: Writing to this register resets V1495 to a default state.

Event FIFO memory data format

Below is format of FIFO event data written for each trigger. Some additional information can be added later. The data readout rate in BLT mode is 20 MB/sec. The actual BLT data length has to be 56 bytes.

31 23 15 7 0

Run number		Firmware type	Data length (bytes)
Status register		Trigger ID	
Majority Logic Setup register		Trigger mask register	
0x00	GPS Coarse Time counter [23:0], (sec.)		
GPS Fine Time counter [31:0], (20 ns)			
GPS One Second counter [31:0], (20 ns)			
TPC Trigger Pattern (TP) [31:0]			
0x000000			TPC TP [39:32]
Trigger counter [31:0]			
0x00	0x00	0x00	0x19
Total trigger inhibit time (µS)			
Trigger inhibit time for the previous trigger (20 ns)			
Live time for the current trigger (20 ns)			
CAEN VME bug data			

Note: Firmware type is 8-bit value, which includes firmware revision bits [11:8] and V1495 board type bits [15:12]. Additional 32-bit word generated by the CAEN VME interface can be safely ignored, but has to be read out.

Ports designation for the *current version* of the V1495 firmware (V1495 Main, v1):

- Port A [31..0] - LVDS, TPC trigger inputs
- Port B [7..0] - LVDS, TPC trigger inputs
- Port C [7..0] - LVDS, Trigger Ordinal (8 bit) output
- Port C [15..8] - LVDS, Trigger Ordinal (8 bit) output
- Port D0 - ECL, TDC clock signal - 40 MHz (PLL generated) output
- Port D1 - ECL, TPC Trigger request output
- Port D2 - ECL, Clock signal - 100 MHz output
- Port E4 - TTL, Test trigger input
- Port E3 - TTL, Memory Full OR from ADCs input

- Port E2 - TTL, Memory Full OR from ADCs input
- Port F7 - TTL, external clock output
- Port F6 - TTL, Run Enable output
- Port F5 - TTL, Run Enable output
- Port F4 - TTL, Memory Full output
- Port F3 - TTL, ADC acquisition window output
- Port F2 - TTL, Trigger output
- Port F1 - TTL, Trigger output
- Port F0 - TTL, Trigger output
- Port G0 - TTL, External clock input
- Port G1 - TTL, 1PPS signal input