

darkside

two-phase argon TPC for Dark Matter Direct Detection



DS-50 Trigger Logic

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Trigger sources

- TPC trigger based on:
 - 38 TPC scintillation counters
- Veto Cherenkov Water (CW) counter and Scintillator Counter (SC) triggers based on:
 - 110 Veto neutron detector counters
 - 80 Veto muon detector counters
- Laser trigger
- Test trigger

TPC Trigger Logic

Majority logic implemented in CAEN V1495 General Purpose VME Board has the following features:

- Number of channels (two spares) - 40
- Signal level - LVDS
- Minimum signal width - 5 ns
- Channel mask register [+] - 40 bits
- Time window (min, max, step) [+] - 10ns, 150ns, 10ns
- Majority trigger low threshold [+] - 1...39
- Majority trigger high threshold [+] - 1...39
- Trigger bit pattern - 40 bits

[+] - Parameters are programmable via VME

V1495 Hardware



- User customizable FPGA Unit (with preloaded demo code)
- Altera Cyclone EP1C20F400C6 FPGA with 32 KB memory
- LVDS/ECL/PECL inputs (differential)
- 64 inputs, expandable to 162 (with 32 outputs)
- 32 outputs, expandable to 130 (with 64 inputs)
- 405 MHz maximum frequency supported for registered logic
- Built-in VME Interrupter logic
- 32-bit BLT data transfer
- I/O delay smaller than 15 ns (in Buffer Mode)
- Programmable 3-color LED
- Libraries (C and LabView) and Software tools for Windows and Linux

Clock Fanout Module (CFM)



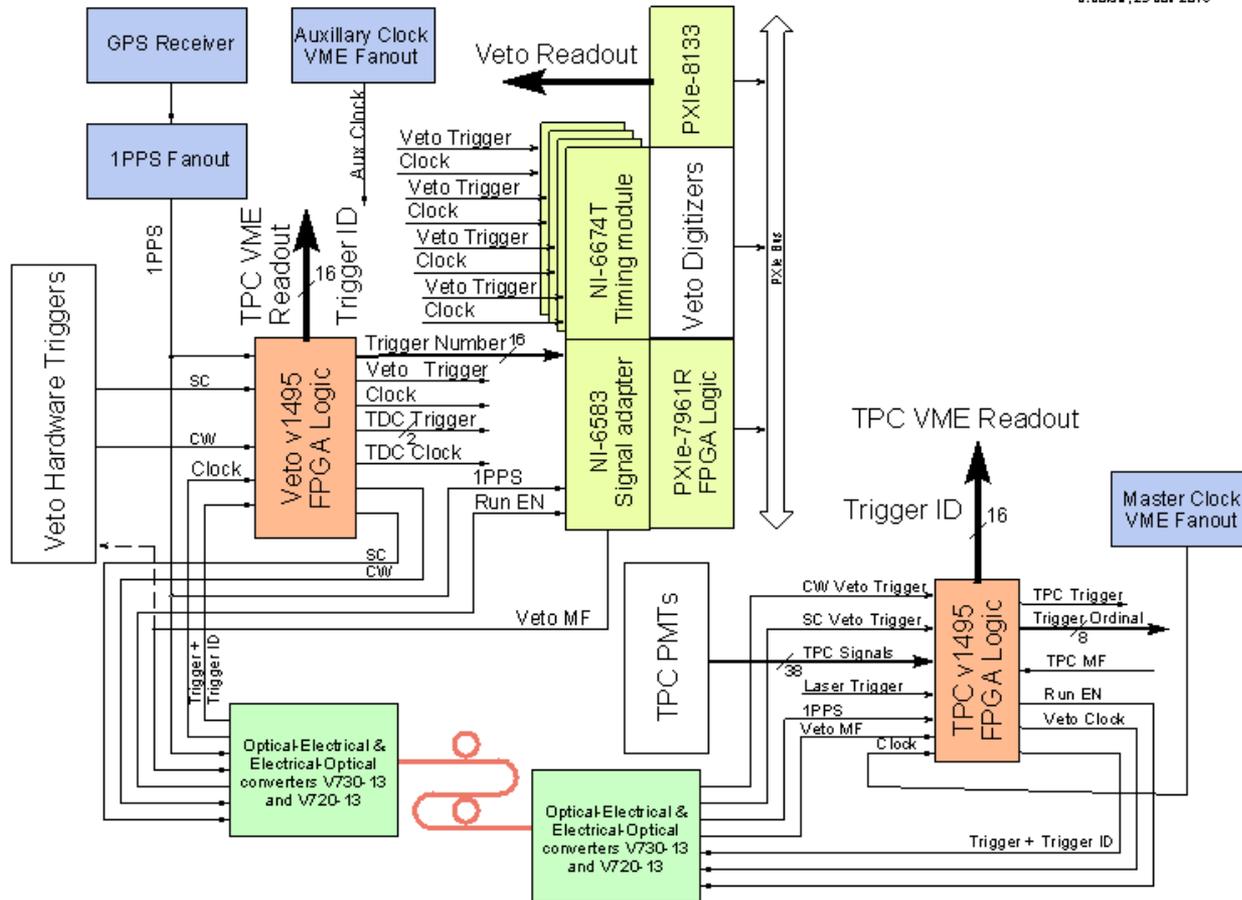
- The LVDS Clock Fanout Module is used to provide high accuracy clock source for DS-50 DAQ and trigger logic
- A single width 6U VME module has the following features:
 - Inputs TTL/LVDS
 - Termination 50 ohm/10K
 - Outputs TTL/NIM/LVDS
 - Output delay (external mode) 20 ns
 - LVDS outputs skew ± 50 ps
 - LVDS output transition 1 ns
 - Number of LVDS outputs 20
 - Output frequency (PLL mode) 190 kHz – 167 MHz
 - Frequency stability ± 5 ppb
 - Front panel LED indicators “Ext.”, “TTL”, “+5V”, “-12V”
 - Jumper selectors “50 ohm/10K”, “Ext./Int.”, “TTL/LVDS”
 - Power consumption +5V – 1.3A
-12V – 0.05A

Global Trigger Concept

- Global Trigger logic provides mechanism to synchronize TPC DAQ and Veto DAQ events
- Global Trigger logic prevents trigger overlap in digitizing ADCs
- Common 50 MHz high accuracy clock allows GPS based timing synchronization of the events
- Both systems can run independently with their own triggers in local mode

Global Trigger Logic

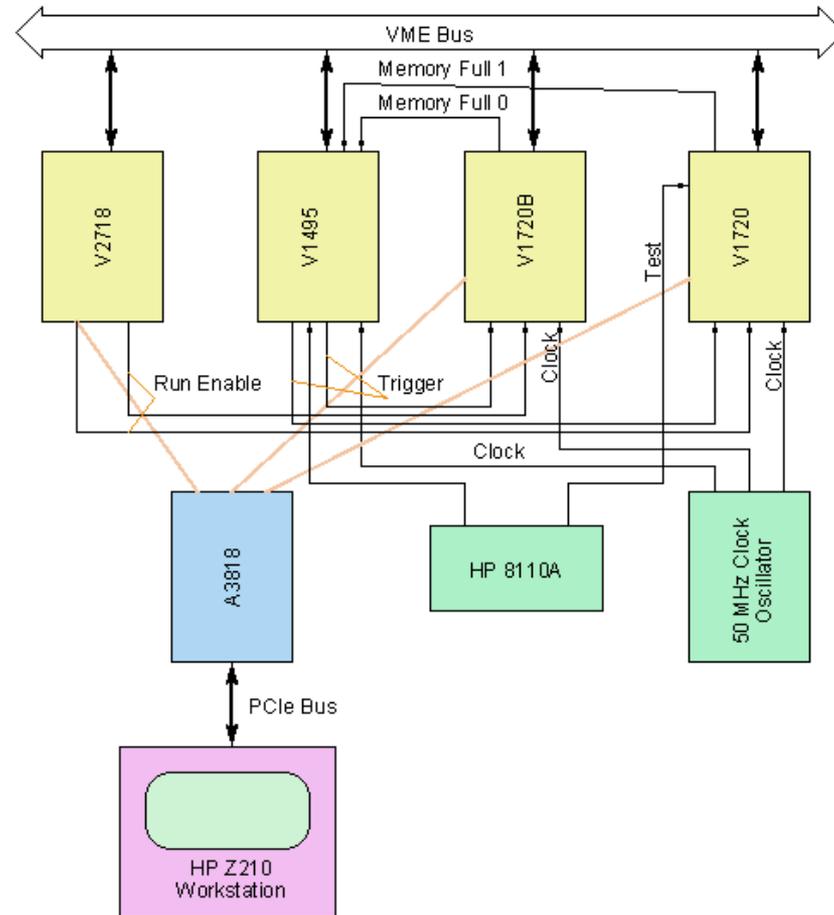
B. Bakti, 29-Jan-2013



TPC Memory Full Study

- V1720 ADC generates a Memory Full (Busy) signal when all internal memory is filled up
- If a trigger is sent to the ADC at this time it will reject it
- Memory Full signals from all ADCs have to be used to prevent this situation
- Additional trigger inhibit has to be provided for the duration of the ADC data acquisition window to prevent trigger overlap
- New CAEN firmware for V1720 tested

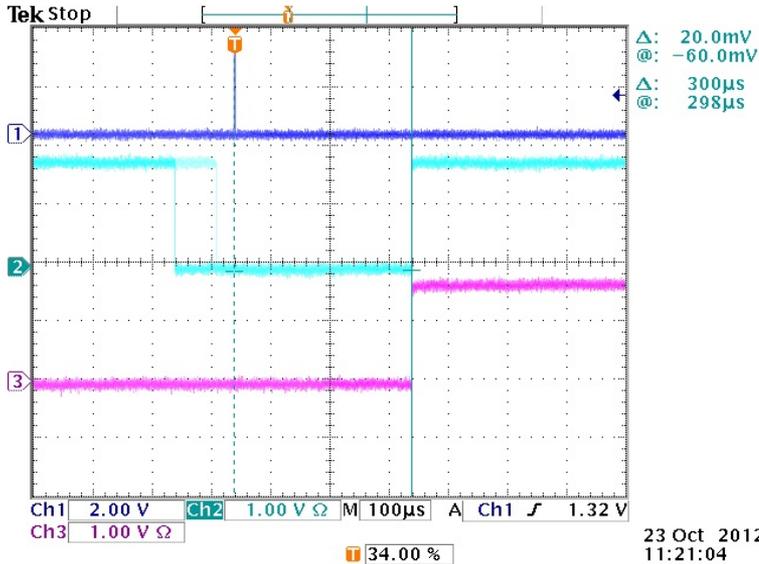
TPC Memory Full Setup



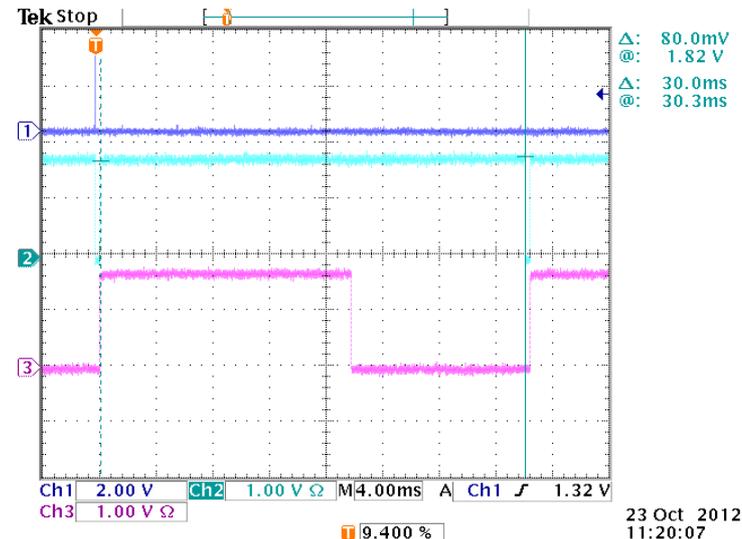
TPC Memory Full Test

- Modified version of Ben's DS10 daqman code (mftest_v1-1)
- V1720B and V1720 ADCs set to 8 buffers
- Acquisition window set to 300 μ S
- External 50 MHz quartz clock source
- External Run Enable signal
- V1495 trigger logic preventing trigger overlap
- Variable trigger rate from HP 8110A pulser (1 Hz - 1 MHz)

TPC Memory Full signal



Trigger signal (Ch1), Memory Full signal ADC1 (Ch2) and Memory Full signal ADC2 (Ch3). The ADC2 (Ch3) releases Memory Full signal after it has been read out. The trigger are not allowed yet since ADC1 is still busy.



TPC Memory Full Study Results

- Stable configuration of the Memory Full logic firmware has been tested and finalized
- Trigger inhibit for the duration of the ADC's acquisition window is required for error free operation
- New CAEN firmware allows easy combining of the Memory Full signals
- Event Counter register of the V1720 is a good tool to verify event synchronization

TPC DAQ Test Stands at Fermilab



TPC DAQ test stand:

- V1495
- Clock Fanout Module
- Two V1720B CAEN ADCs
- 64-bit Fragment Receiver and Event Builder

DS-50 Trigger test stand:

- Two V1495 modules
- Clock Fanout Module
- V1720B and V1720 CAEN ADCs
- HP Z210 Workstation (32-bit)



Trigger Development Flow

- TPC Memory Full logic (done)
- TPC majority logic (done)
- Test pattern generator (done)
- Event FIFO implementation (in progress)
- GPS event timing (in progress)
- Interrupt logic implementation (in progress)
- V1495 serial communication
- Hardware testing

Trigger Development Schedule

- TPC local trigger February 24
- Veto local trigger April 30
- Veto timing fanout April 30
- DS-50 Global trigger May 15

References

1. Stefano Davini et al., “Electronics and Data Acquisition system for the DarkSide50 Veto”, DarkSide Document 480-v2, 12 Dec 2012
2. CAEN S.p.A., “V1495 General Purpose VME Board”, <http://www.caen.it/csite/CaenProd.jsp?parent=1&idmod=704>
3. B.Baldin, “DS50 Clock Fanout Module”, DarkSide Document 471-v2, 11 Dec 2012
4. B.Baldin et al., ”Study of the Memory Full signals of CAEN V1720 ADCs”, DarkSide Document 460-v4, 14 Jan 2013
5. B.Baldin et al., “Global trigger system for the DarkSide-50 experiment”, DarkSide Document 485-v1, 24 Dec 2012,