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New Firmware for CAEN V1720 ADC

We have received a new version of the firmware for the V1720 ADC and tested it. The new firmware allows independent programming of the LVDS I/O port in groups of four channels. Each group can be used for pattern, trigger or programmed I/O functions. A description of the new functionality is provided in CAEN note "VME Digitizers: Front Panel LVDS signals, new features". The Trigger Ordinal 8-bit value can now be implemented along with Memory Full OR scheme that allows chaining multiple ADCs Memory Full (Busy) signals in a single TTL signal at the TRG OUT LEMO connector. Below is a description of the V1495 MF_logic firmware registers and required ADC settings for using the new firmware. The V1495 MF_logic firmware was tested with the input trigger rates up to 1 MHz and demonstrated stable operations. The default base address of the V1495 module is 0x01000000.

Run Control register

Address: Base + 0x1018
Size: 32 bit
Mode: R/W

Bit	Function	Default
[0]	Run Enable, 1 - enable	0
[1]	Memory Full Inhibit enable, 1 - enable	0
[2]	Extension of the MF signal enable , 1 - enable	0
[3]	Reserved	
[4]	Pause run, 1 - pause	
[15:5]	Reserved	0
[31:16]	Internal trigger frequency 1 Hz – 65 kHz, 0 - disable	0

Note: Write 0x3 or 0x7 to this register to start the run, write 0x0 to stop the run.
Bit [4] can be used for disabling triggers. The triggers are disabled when the bit is set to 1.
Bit [16] corresponds to ~ 1 Hz, bit [31] corresponds to ~ 65 kHz.
Only one bit of the frequency setting can be set at a time.
If none of the bits is set (all zero) the internal pulser is disabled.

ADC Data Acquisition Window Inhibit register

Address: Base + 0x101C
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	ADC data acquisition window, 20 ns step	0x00003C8C

Note: This setting must exceed the actual ADC data acquisition window by a few microseconds.

MF Extension Inhibit register

Address: Base + 0x1020
Size: 32 bit
Mode: R/W

Bit	Function	Default
[31:0]	MF Extension pulse duration, 20 ns step	0x 00000032

Note: This setting currently is not used, but left for additional functionality.

The following settings are necessary for running CAEN ADCs in the new firmware mode:

- Write 0x000D0151 to the address 0x811C
- Write 0x0 to the address 0x816C
- Write 0x00002200 to the address 0x81A0
- To start the run write 0x0000010D to the address 0x8100
- To stop the run write 0x00000109 to the address 0x8100
- To pause the run write 0x0000011D to the address 0x8100
- To resume the run write 0x0000010D to the address 0x8100

Note that Event Counter and Trigger Time Tag registers will be reset every time bit [1] of the Run Control register in V1495 transitioned from zero to one. The DAQ software has to verify that the Trigger Ordinal (8-bit) in the ADC header matches the Event counter in the same ADC event buffer as well as in the data headers of all other ADCs for the same event. Additional information in case of mismatch can be obtained from the Trigger Time Tag register in the headers.

Ports designation for the *current version* of the V1495 firmware (MF_logic):

- Port C [7..0] - Trigger Ordinal (8 bit)
- Port C [15..8] - Trigger Ordinal (8 bit)
- Port F7 - TTL, external clock output
- Port F6 - TTL, Run Enable output
- Port F5 - TTL, Run Enable output
- Port F4 - TTL, Memory Full input
- Port F3 - TTL, Memory Full output
- Port F2 - TTL, Trigger output
- Port F1 - TTL, Trigger output
- Port F0 - TTL, Trigger output
- Port G0 - TTL, External clock input
- Port G1 - TTL, External trigger input