



VME Digitizers: Front Panel LVDS signals, new features.

Preliminary

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1 New Features

On VME CAEN Digitizer, from the ROC FW revision 3.8, a new configuration mode for LVDS signal is present. Previous configurations are still available.

The new configuration mode allows to select the direction (IN/OUT) and the functionality for signals in groups of 4; the available features are described in section 2.1.2

Was also introduced the possibility of having the BUSY signal on the TRGOUT connector.

1.1 Busy signal

The generated **Busy** signal (out on LVDS or LEMO connector) is

Busy = Almost_Full or (LVDS_BusyIn and BusyIn_enable)

where

- Almost_Full: Indicates the filling of the Buffer Memory up to a programmable level (**see 2.1.4**)
- LVDS_BusyIn : available in nBUSY/nVETO configuration (**see 2.1.2**)
- BusyIn_enable: bit8 of Acquisition Control register (**see 2.1.3**)

2 Registers

We report here only the registers related to the New LVDS Feature. For the other board registers refer to the V17xx User's Manual.

2.1 Registers content

2.1.1 Front Panel I/O Control Register

Address: 0x811C,
Bits: [31:0]
Access Mode: Read and Write

[0]	Front Panel logic level: 0 = TRG/CLK are NIM I/O Levels 1 = TRG/CLK are TTL I/O Levels
[1]	0= panel output signals (TRG-OUT/CLKOUT) enabled 1= panel output signals (TRG-OUT/CLKOUT) enabled in high impedance
[2]	0 = LVDS I/O 3..0 are inputs 1 = LVDS I/O 3..0 are outputs
[3]	0 = LVDS I/O 7..4 are inputs 1 = LVDS I/O 7..4 are outputs
[4]	0 = LVDS I/O 11..8 are inputs 1 = LVDS I/O 11..8 are outputs
[5]	0 = LVDS I/O 15..12 are inputs 1 = LVDS I/O 15..12 are outputs
[7:6]	LVSD signal configuration (old features: bit 7:6 are meaningful only if bit8 = 0) 00 = General Purpose I/O 01 = Programmed I/O 10 = Pattern mode: LVDS signals are input and their value is written into header PATTERN field.
[8]	LVSD signal: new features select: 0 = LVDS old features 1 = LVDS new features
[13:9]	Reserved, all must be 0
[14]	1= TRG-OUT Test Mode set to 1 0 = TRG-OUT Test Mode set to 0
[15]	0 = I/O Normal operations: TRG-OUT signals outside trigger presence (trigger are generated according to Front Panel Trigger Out Enable Mask setting, see § 4.24) 1= I/O Test Mode: TRG-OUT is a logic level set via bit 14
[17:16]	TRGOUT mode select 00 = Trigger 01 = Motherboard probes (see bit [19:18]) 10 = Channels probes 11 = SIN propagation
[19:18]	Motherboard Probe select 00 = RUN 01 = CLKOUT 10 = CLK phase 11 = BUSY
[31:20]	Reserved

2.1.2 Front Panel LVDS I/O New Features Register

Address: 0x81A0
Bits: [15:0]
Access Mode: Read and Write

[3:0]	LVDS I/O 3..0 configuration
[7:4]	LVDS I/O 7..4 configuration
[11:8]	LVDS I/O 11..8 configuration
[15:12]	LVDS I/O 15..12 configuration

The possible configurations are:

- 0000 = REGISTER
- 0001 = TRIGGER
- 0010 = nBUSY/nVETO
- 0011 = OLD STYLE.

Features description when LVDS group is configured as INPUT

	REGISTER*	TRIGGER	nBUSY/nVETO	OLD STYLE
LVDS IN [3:0]	Reg[3:0]	TriggerIn_Ch[3:0]	3:nRunIn 2:nTriggerIn 1:nVetIn 0:nBusyIn	3:reserved 2:reserved 1:reserved 0:nClear_TTT
LVDS IN [7:4]	Reg[7:4]	TriggerIn_Ch[7:4]	7:nRunIn 6:nTriggerIn 5:nVetIn 4:nBusyIn	7:reserved 6:reserved 5:reserved 4:nClear_TTT
LVDS IN [11:8]	Reg[11:8]	TriggerInt_Ch[3:0]	11:nRunIn 10:nTriggerIn 9:nVetIn 8:nBusyIn	11:reserved 10:reserved 9:reserved 8:nClear_TTT
LVDS IN [15:12]	Reg[15:12]	TriggerIn_Ch[7:4]	15:nRunIn 14:nTriggerIn 13:nVetIn 12:nBusyIn	15:reserved 14:reserved 13:reserved 12:nClear_TTT

*) Front Panel I/O Data Register (address 0x8118) allows to readout the logic level of LVDS I/Os.

Features description when LVDS group is configured as OUTPUT

	REGISTER**	TRIGGER	nBUSY/nVETO	OLD STYLE
LVDS OUT [3:0]	Reg[3:0]	TriggerOut_Ch[3:0]	3:nRun 2:nTrigger 1:nVeto 0:nBusy	3:Run 2:Trigger 1:DataReady 0:Busy
LVDS OUT [7:4]	Reg[7:4]	TriggerOut_Ch[7:4]	7:nRun 6:nTrigger 5:nVeto 4:nBusy	7:Run 6:Trigger 5:DataReady 4:Busy
LVDS OUT [11:8]	Reg[11:8]	TriggerOut_Ch[3:0]	11:nRun 10:nTrigger 9:nVeto 8:nBusy	11:Run 10:Trigger 9:DataReady 8:Busy
LVDS OUT [15:12]	Reg[15:12]	TriggerOut_Ch[7:4]	15:nRun 14:nTrigger 13:nVeto 12:nBusy	15:Run 14:Trigger 13:DataReady 12:Busy

**) The Front Panel I/O Data Register (address 0x8118) allows to set the logic level of LVDS I/Os.

2.1.3 Acquisition Control

Address: 0x8100
 Bits: [31:0]
 Access Mode: Read and Write

[0:1]	00 = REGISTER-CONTROLLED RUN MODE 01 = S-IN CONTROLLED RUN MODE 10 = S-IN GATE MODE 11 = MULTI-BOARD SYNC MODE
[2]	0 = Acquisition STOP 1 = Acquisition RUN allows to RUN/STOP Acquisition
[3]	0 = COUNT ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS allows to reject overlapping triggers (see § 3.3.3)
[7:4]	reserved
[8]	0 = LVDS BusyIn disabled 1 = LVDS BusyIn enabled
[9]	0 = LVDS VetoIn disabled 1 = LVDS VetoIn enabled
[31:10]	reserved

2.1.4 Memory Buffer Almost Full Level register

Address: 0x816C,
 Bits: [11:0]
 Access Mode: Read and Write

This register allows setting the level for Almost_Full generation. If this register is 0, the Almost_Full is a Full.