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# Global trigger system for the DarkSide-50 experiment

(Technical specification)

## 1. Introduction

The DAQ system of the DarkSide-50 experiment includes TPC digitizers and Veto digitizers. The TPC DAQ uses CAEN V1720 modules and the Veto system uses NI PXIe-5162 modules. The main difference between uses of the two digitizers is the width of the selected data acquisition window. For the PXIe-5162 it is between 1 µS and 60 µS, while for the V1720 it is about 300 µS or more. It is *absolutely necessary* to synchronize two types of digitizers with the TPC trigger, so full background information will be available for each TPC event. It is assumed below that NI PXIe-5162 digitizer behaves similarly to the CAEN V1720 in terms of event buffering and triggers overlap.

The following terminology is used in this document:

- There are four FPGA-based trigger logic units in the DS-50 DAQ system:
  - TPC V1495 trigger module located at the TPC site (clean room)
  - Veto V1495 trigger module located at the Veto site (control room)
  - Veto Fanout V1495 module located at the Veto site (control room)
  - Veto FPGA logic module located in the PXIe crate at the Veto site (control room)
- Unless otherwise noted, signals in the block diagram are active high TTL, ECL or LVDS
- NI modules mentioned in this document are just possible examples, which provide required functionality for the Veto system

## 2. Trigger logic scheme

The following scheme (Figure 1) is proposed to satisfy the above synchronization requirement. The Hardware Veto Trigger signals are sent via optical links to the TPC V1495 trigger module located at the TPC site. Currently there are two types of Hardware Veto triggers: Scintillation Counter (SC) trigger and Cherenkov Water detector (CW) trigger. The TPC V1495 module generates *all the triggers* for the experiment. The trigger signal and 16-bit Trigger ID are transferred via optical link back to the Veto V1495 trigger module located at the Veto system site. The trigger ID consists of two parts: 12-bit Trigger Number and 4-bit Trigger Type. The logic inside Veto V1495 trigger module decodes Trigger ID and places it in an internal FIFO memory for the readout via VME bus as a part of the TPC data stream. The same Trigger ID and the trigger signal are also available for the Veto DAQ readout via digital adapter module NI 6583 attached to FlexRIO FPGA PXIe-7961R module. The FlexRIO FPGA PXIe-7961R module is similar to the CAEN V1495 module and allows user to implement desirable trigger logic in the on-board

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FPGA. The depth of the corresponding FIFO memory for storing Trigger ID information *should not exceed the number of buffers* allocated in the sampling ADCs in each DAQ sub-system. A 50 MHz clock signal is also sent to the Veto site for synchronization of both Veto and TPC ADCs to the same clock frequency. Both V1495s and the Veto system FPGA logic module also receive 1PPS signal from the LNGS GPS receiver.

Triggers arriving at the Veto V1495 trigger module are dedicated for the Veto digitizers and TDCs. A delayed trigger signal (TDC trigger) for the TDC modules located at the Veto site is generated by the Veto V1495 trigger module. In order to manage high trigger rates, the Memory Full signals of the V1720 ADCs are ORed and used to inhibit TPC triggers when there are no memory buffers available. A similar Memory Full signal is derived by the FlexRIO FPGA PXIe-7961R module in the Veto DAQ system in order to keep data readout rate at the maximum. This signal is sent to the TPC site to prevent generation of the TPC trigger (and associated Veto triggers) when the Veto system is busy. Optionally this signal could also be used locally to block Hardware Veto triggers (dashed line). The FlexRIO FPGA PXIe-7961R module has internal memory which can be used as a FIFO memory to store Trigger ID and GPS timestamps for each incoming Veto trigger. This memory should be read out with each event in order to provide a trigger marker for event synchronization.

The TPC V1495 trigger module has to generate appropriate dead time for each trigger type equal to the data acquisition window thus preventing trigger overlap within it. In addition, the TPC trigger will not be issued, if the Veto system is processing (1 to 60 µS) the previous trigger. The Veto triggers will be generated at the desired rate and each Veto trigger type will have a unique Trigger Number. The TPC V1495 trigger module will increment the Trigger Number when any trigger type is generated. When the TPC trigger is generated, the Trigger Number sent to the Veto system with each trigger will not be incremented within TPC data acquisition window. This will mark all Veto events within that window with the *same Trigger Number* (but different Trigger Type) and will allow easy event synchronization. Additionally, the lower eight bits of the Trigger Number are sent to the V1720 I/O connectors. This 8-bit number is called TPC Trigger Ordinal.

## *Signals shown in the DS-50 Global Trigger logic block-diagram:*

- Run EN is Run Enable signal (called S-IN in CAEN documentation) used in the TPC system to start data sampling ADCs. This is a level TTL signal, HIGH means run enabled. This signal should be used to synchronize start and stop of the run in the Global trigger mode.
- Auxiliary Clock Fanout Module can be used to run Veto system when the TPC V1495 module is down. The Veto V1495 trigger module will use one of the two clock sources whichever is connected to the port G0 Lemo connector (manual switching of the cable required).
- The Veto Hardware trigger signals are LVDS level signals and have to be converted by the Veto V1495 trigger module to TTL. These signals also will be used directly by the Veto system when running in the Local mode. A local Trigger ID will be provided by the Veto V1495 trigger module in this case. A delay adjustment of the pre-trigger window will be required.
- A 1PPS signal is fanned out using a TTL fanout module (e.g. NIM module) located in the control room

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- The Veto Fanout V1495 module provides four copies of 1PPS, Run Enable, 50 MHz clock and trigger signals for the Veto system's FPGA and timing modules, and receives Veto Memory Full and Veto DAQ error signals (only Veto MF shown).

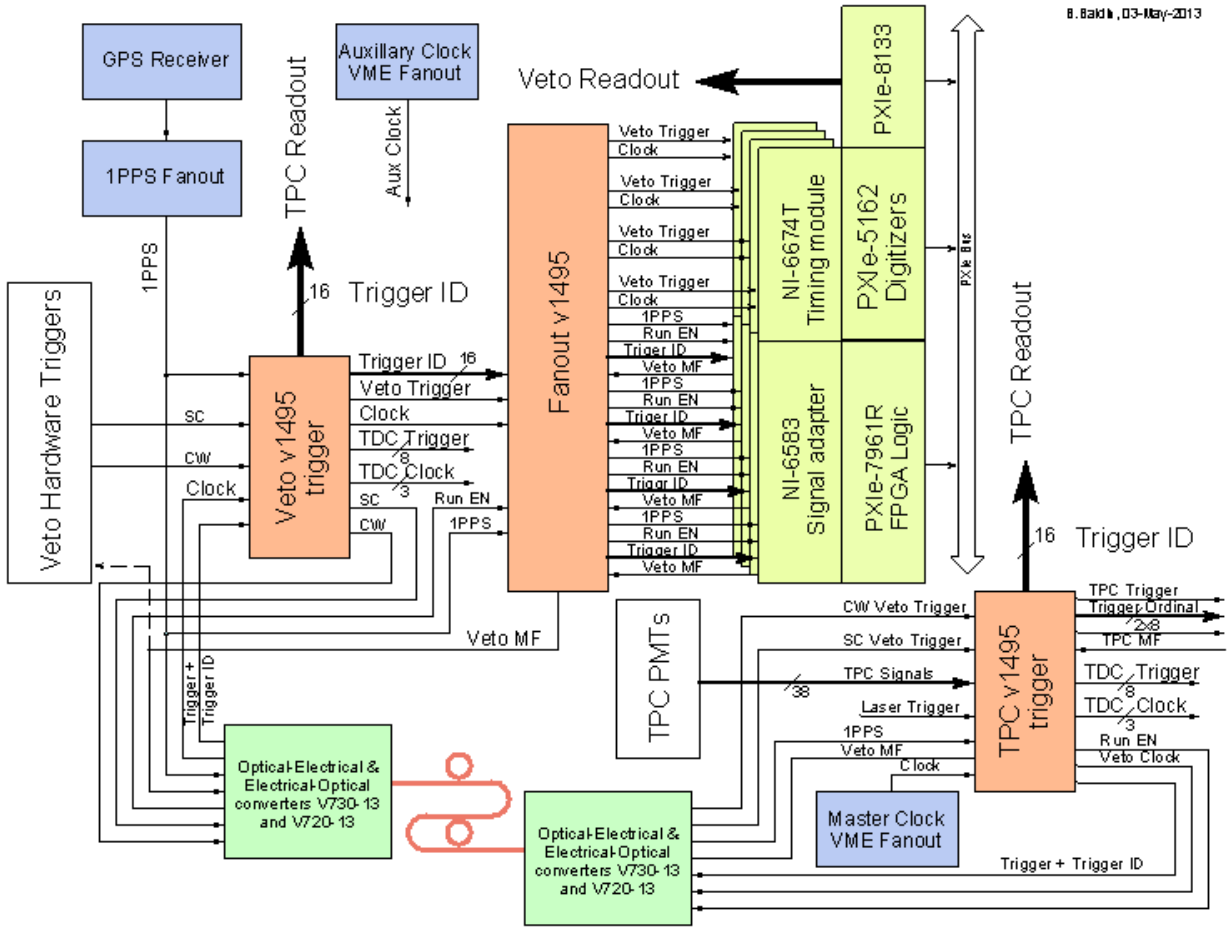


Figure 1. DS-50 Trigger logic

## 3. Trigger inhibit logic

As described in the DS-50 note 460-v3, it is necessary to inhibit triggers for the time when any ADC's memory is full. This is currently implemented by using chained OR of the ADC Memory Full signals using new V1720 firmware in TPC ADCs (see DS-50 note 491-v2). A similar signal will be generated by the NI PXIe-7961R module and used by the TPC V1495 trigger module (without this signal it is not possible to guarantee event synchronization between two sub-systems). In addition, generation of any trigger type will be inhibited for the appropriate time after the trigger was issued. The inhibit time settings for two trigger types are the following:

- Veto trigger - 1…60 µS
- TPC trigger - 10…500 µS

The TPC V1495 trigger output is enabled synchronously with the Run Enable signal controlled by a bit in the VME register. The Veto system receives Run Enable signal from the TPC V1495 trigger module and will use it to control and synchronize its DAQ.

## 4. Modes of operation

It is assumed that two sub-systems will run independently at some times collecting data with their own triggers. For that reason two modes of operation are envisioned:

- Local mode in which each sub-system receives and records only its own triggers.
- Global mode as described above.

The following logic (simplified) is implemented in the TPC V1495 trigger module for the Global trigger mode (priority high to low):

- If any trigger inhibits or memory full signals are present, wait. Otherwise, go to the next step.
- If any trigger requests are present, generate appropriate trigger and go to the previous step.

The following figures illustrate various modes of operation. The local TPC trigger mode is shown in Figure 2 below. The TPC_TIN signal represents TPC trigger generated by the majority logic. Note that Memory Full signal and trigger inhibit signal (TPC_INH, equal or longer than ADC acquisition window) have to overlap. This can be achieved by appropriate programming of the duration of the TPC_INH using corresponding VME register.

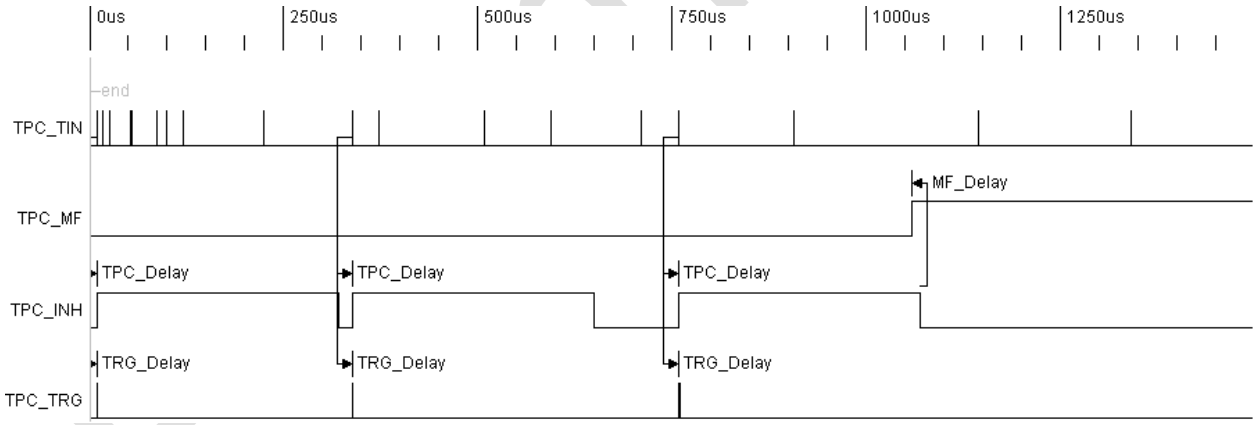


Figure 2. TPC local trigger mode

The Veto local mode is illustrated in Figure 3 below. The VETO_TIN signal represents an OR of CW and SC Veto triggers. The same overlap requirement for the Veto Memory Full signal is true.

One example of possible interaction between TPC and Veto DAQ systems is shown in Figure 4 below. Note that only two out of three Veto triggers are recorded by the Veto system for the second TPC trigger. This is due to the requirement of having independent Veto triggers in parallel with the TPC triggers while in the global trigger mode. The probability of this happening can be reduced if the Veto

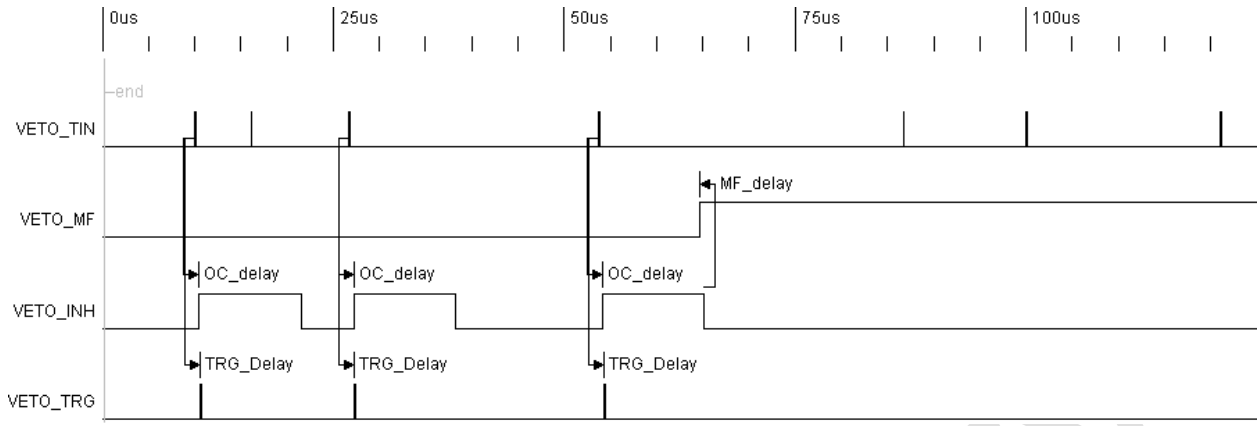


Figure 3. Veto local trigger mode

system will be allowed to record only triggers related to the TPC trigger (i.e. within TPC acquisition window). Chance of getting Memory Full signal in this case is much less, but not zero either. Full elimination of the Veto trigger losses is possible only if both systems have common readout scheme. The presence of the Veto Memory Full signal during TPC acquisition window will be recorded and included in the TPC Event FIFO data.

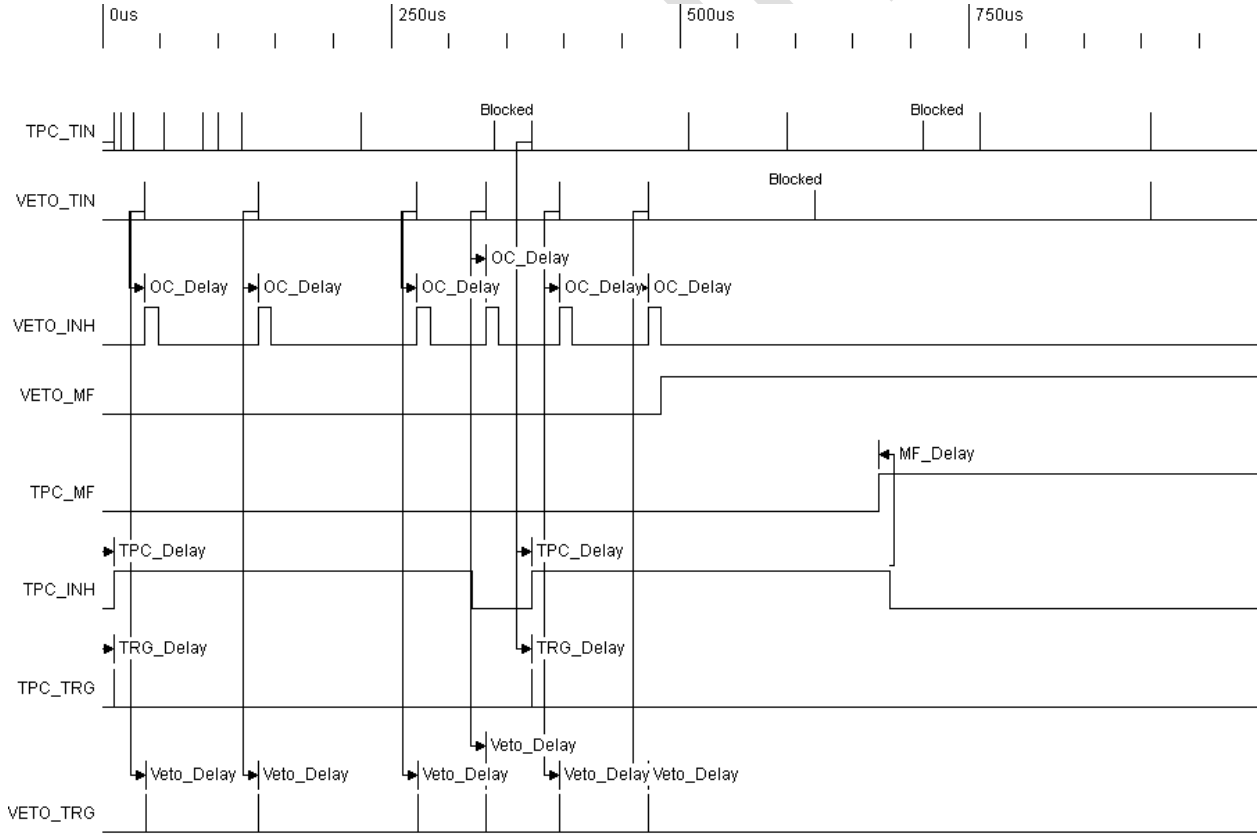


Figure 4. Global trigger mode

## 5. GPS timing using 1PPS signal

A 1PPS signal will be used by all three FPGA logic units as the following:

- Each unit will have a 32-bit counter to count 50 MHz pulses between 1PPS pulses to provide fine GPS time stamp
- Each unit will have a 24-bit counter to count 1PPS pulses to provide coarse 1 sec time stamp
- Both counters will be stored in the event FIFO when a trigger is generated and read out with each event

## 6. TPC trigger logic

The following is a preliminary description of the majority logic for the TPC detector system. The current parameters are used for the design of the FPGA firmware and can be modified as necessary (parameters marked with [+] are programmable via VME):

- Number of channels (two spares) - 40
- Signal level - LVDS
- Minimum signal width - 5 ns
- Channel mask register [+] - 40 bits
- Time window for all channels (min, max, step) [+] - 10ns, 150ns, 10ns
- Majority trigger low threshold [+] - 1...39
- Majority trigger high threshold [+] - 1...39
- Trigger bit pattern - 40 bits

## 7. Event information stored in the TPC V1495 FIFO memory

The following are preliminary parameters stored in the FIFO memory (Event FIFO) for each trigger generated for the TPC system. The Veto system has to store at least 16-bit Trigger ID and two GPS counters described above.

Table 1. TPC FIFO data for each event

| FIFO Data | # Bits | Meaning | Source |
|---|---|---|---|
| Data length | 8 | FIFO event length (bytes) | Firmware |
| Firmware type | 8 | Firmware type | Firmware |
| Run Number | 16 | Run number stored in the V1495 register | DAQ |
| Trigger ID | 16 | Trigger number + Trigger type | Firmware |
| Status register | 16 | Various status and error bits | Firmware |
| Trigger mask | 32 | Majority logic settings and Trigger mask bits | Firmware |
| GPS-CT | 24 | Coarse time of GPS signal (seconds) | Firmware |
| GPS-FT | 32 | Fine time of GPS signal (clock cycles) | Firmware |
| GPS-1S | 32 | Time between 1PPS pulses (clock cycles) | Firmware |
| CPAT | 40 | Active elements in trigger | Firmware |
| Total_trig | 32 | Total number of triggers in the run | Firmware |
| SC_Veto_sent | 8 | Number of SC Veto triggers in the event | Firmware |

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|---|---|---|---|
| CW_Veto_sent | 8 | Number of CW Veto triggers in the event | Firmware |
| SC_Veto_rcvd | 8 | Total number of SC Veto triggers during the event | Firmware |
| CW_Veto_rcvd | 8 | Total number of CW Veto triggers during the event | Firmware |
| Dead_time_total | 32 | Total duration of the trigger inhibit active [µS] | Firmware |
| Dead_time_cur | 32 | Trigger inhibit duration for previous trigger [20 nS] | Firmware |
| Live_time_cur | 32 | Trigger logic input open for current trigger [20 nS] | Firmware |

## 8. Event synchronization in the TPC DAQ system

As designed, the V1720 provides two registers in the event data header: Trigger Time Tag and Event Counter. The Trigger Time Tag is a 32-bit 125 MHz counter latched at the arrival of the trigger. The 24-bit Event Counter has to be programmed to count all incoming triggers. Having this information in each event allows one to identify the events mismatch. The same event recorded by different ADCs should have identical time tag and event count in the header (see Figure 2). Both counters have to be properly synchronized at the beginning of the run, which is guaranteed by using external Run Enable signal. An identical synchronization condition of the ADCs is achieved by using star-like distribution of Clock, Trigger and Run Enable signals to all ADCs with equal delays.

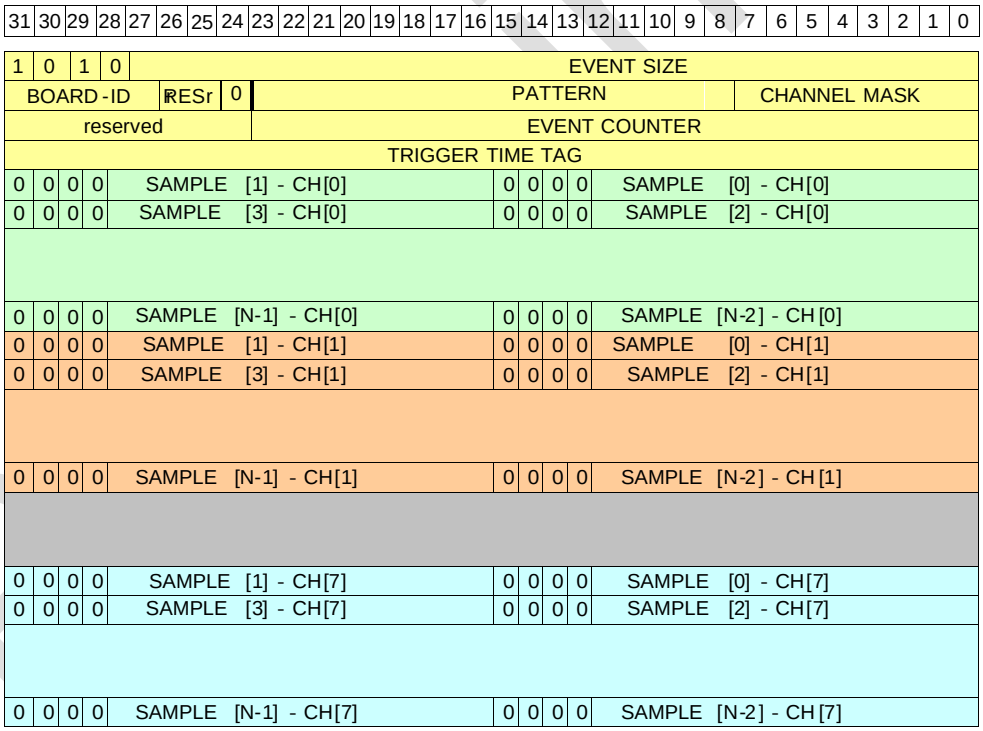


Figure 5. CAEN V1720 event structure

The 2x8-channel V976 fanout module from CAEN will be used to distribute Trigger and Run Enable signals. For the clock distribution LVDS Clock Fanout Module designed by Fermilab will be used. Both Trigger and Run Enable signals are synchronized to the ADC clock by the TPC V1495 trigger module according to the V1720 specification.

In addition to the Event Counter register, an 8-bit copy of lower 8-bits of the Trigger Number (Trigger Ordinal) is provided at the I/O connectors of two ADCs. This number is embedded in the event header read out from these ADCs and can be compared to the Trigger Number stored in the Event FIFO for each event.

## 9. Signal connections to the trigger modules

Below are specifications for the V1495 and Veto system DAQ modules.

### *TPC V1495 trigger module ports designations:*

1. Port A - 32 LVDS input signals:
    a. 30 signals from TPC frond-end boards
    b. Reserved (2)
2. Port B - 32 LVDS input signals:
    a. 10 signals from TPC frond-end boards
    b. Reserved (22)
3. Port C - 32 LVDS output signals:
    a. Trigger Ordinal (8-bits of Trigger ID)
    b. Trigger Ordinal (8-bits of Trigger ID)
    c. 16 - bit Trigger test pattern (programmable)
4. Port D - 32 ECL output signals:
    a. TDC clock (3) - 40 MHz (PLL generated)
    b. TPC Trigger (8)
    c. Reserved (21)
5. Port E – Eight (8) TTL input signals:
    a. CW Trigger
    b. SC Trigger
    c. External Laser Trigger
    d. External TPC Trigger
    e. TPC MF signal (2)
    f. Veto MF signal
    g. Reserved (1)
6. Port F – Eight (8) TTL output signals:
    a. TPC trigger
    b. Veto Clock
    c. Encoded Trigger
    d. Run Enable (2)
    e. Trigger inhibit
    f. TPC Test pulse OR TPC trigger (programmable)
    g. Laser Test pulse OR Test Pattern Strobe (programmable)
7. Port G – TTL input signals:
    a. External clock (50 MHz)

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b. 1PPS signal

### *The Veto V1495 trigger module ports designations:*

1. Port A – 32 LVDS input signals:
    a. CW Veto trigger
    b. SC Veto trigger
    c. Reserved (30)
2. Port B - 32 LVDS input signals:
    a. DAQ error status bit (4)
    b. Memory Full signal (4)
    c. Reserved (24)
3. Port C - 32 LVDS output signals:
    a. 16-bit Trigger ID for the Veto system
    b. Veto trigger
    c. Veto 50 MHz clock
    d. 1PPS signal
    e. Run Enable
    f. Reserved (12)
8. Port D - 32 ECL output signals:
    a. TDC clock (3) - 40 MHz (PLL generated)
    b. TPC Trigger (8)
    c. Reserved (21)
4. Port E - TTL input signals:
    a. Encoded Trigger
    b. External Veto trigger
    c. Run Enable
    d. Reserved (5)
5. Port F - TTL output signals:
    a. Veto trigger (2)
    b. Veto clock
    c. Veto Run Enable
    d. CW trigger
    e. SC trigger
    f. Veto Memory Full
    g. Veto trigger inhibit
6. Port G – TTL inputs:
    a. External clock (50 MHz)
    b. 1PPS signal

### *The Veto Fanout V1495 module ports designations:*

7. Port A – 32 LVDS input signals:

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    a. 16-bit Trigger ID for the Veto system
    b. Veto trigger
    c. Veto 1PPS signal
    d. Veto Run Enable
    e. Veto 50 MHz clock
    f. Reserved (12)
8. Port B - 32 LVDS input signals:
    a. DAQ error status bit (4)
    b. Memory Full signal (4)
    c. Reserved (24)
9. Port C - 32 LVDS output signals:
    a. 16-bit Trigger ID for the Veto system
    b. 16-bit Trigger ID for the Veto system
9. Port D - 32 LVDS output signals:
    a. 16-bit Trigger ID for the Veto system
    b. 16-bit Trigger ID for the Veto system
10. Port E - 32 LVDS output signals:
    a. Veto 1PPS signal(4)
    b. Veto Run Enable (4)
    c. Memory Full signal (4)
    d. DAQ error status (4)
    e. Reserved (16)
11. Port F - TTL output signals:
    a. Veto trigger (4)
    b. Veto clock (4)
12. Port G – TTL inputs:
    a. External clock (50 MHz)
    b. 1PPS signal

### *Veto system DAQ modules ports designations:*

1. NI PXIe-6674T timing modules (4):
    a. External Clock input 50 MHz (TTL)
    b. Veto trigger input (TTL)
2. NI-6583 Signal Adapter modules (4):
    a. 16-bit Trigger ID input (LVDS)
    b. Veto 1PPS signal input (LVDS)
    c. Veto Memory Full signal output (LVDS)
    d. Run Enable signal input (LVDS)

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