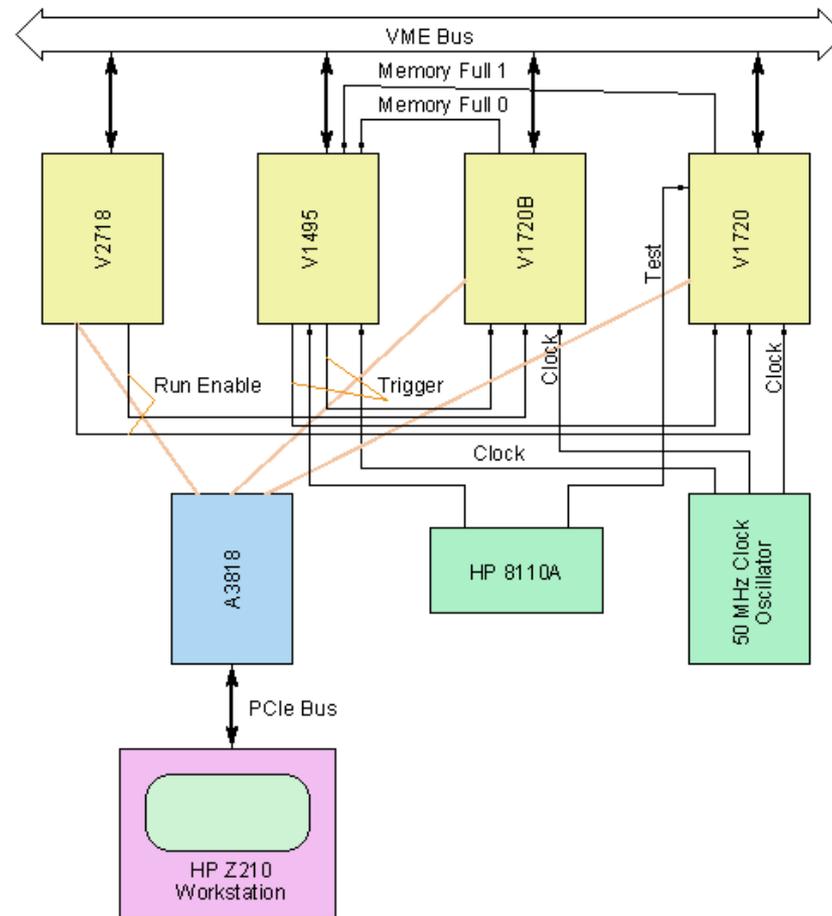


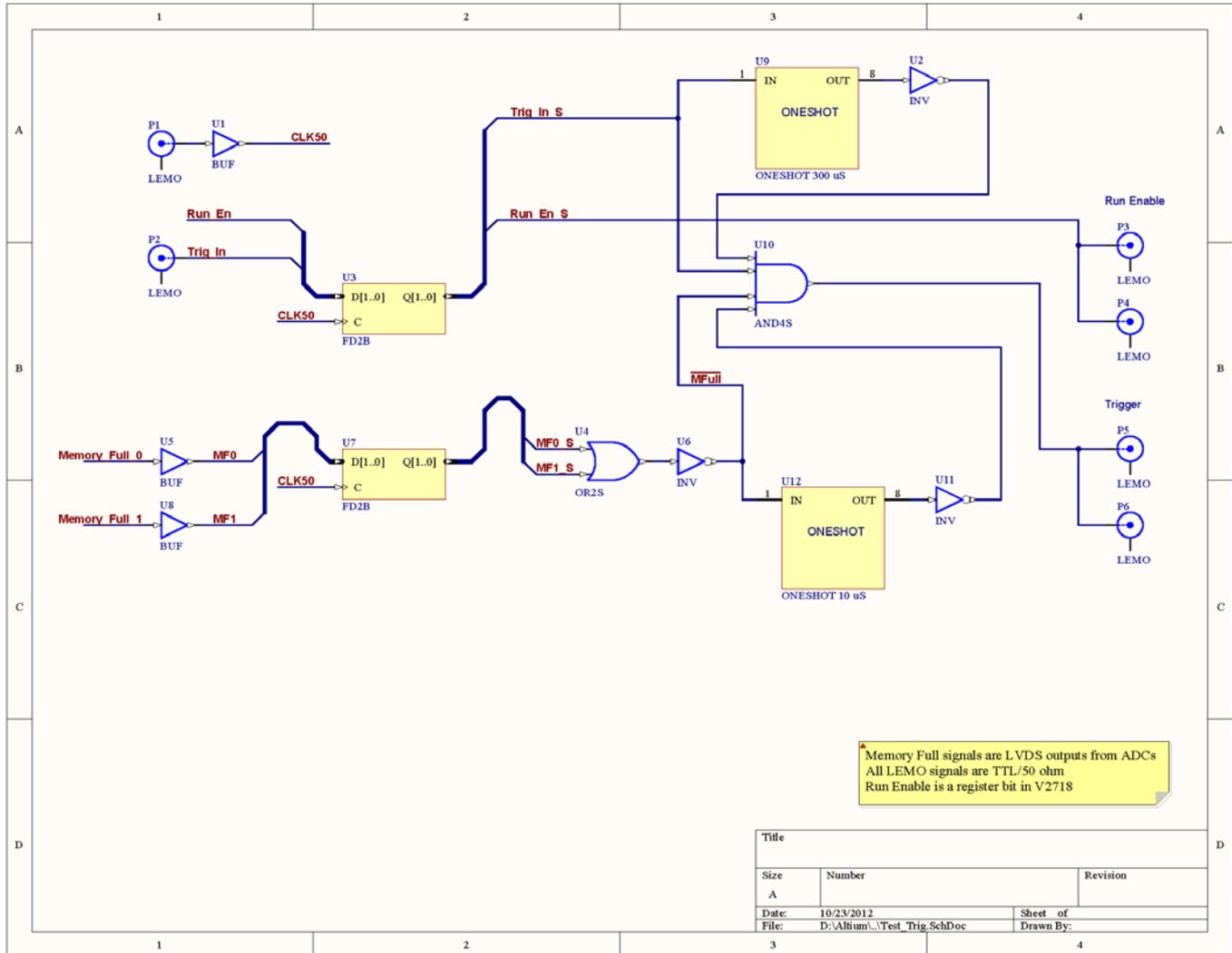
Study of the Memory Full signals of CAEN V1720 ADCs

B.Baldin, B.Loer, J.Wu

Block-diagram of the setup



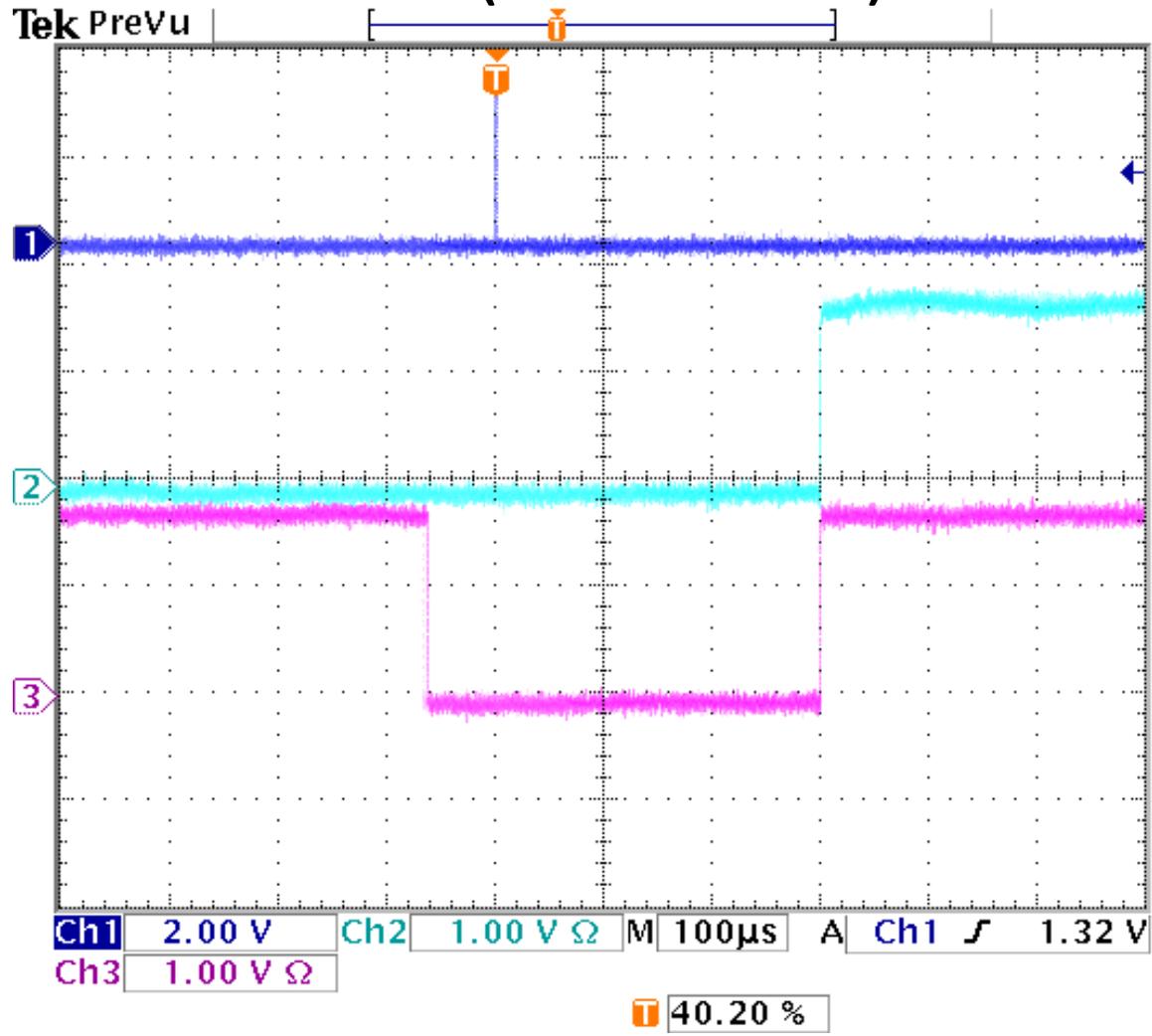
V1495 Logic



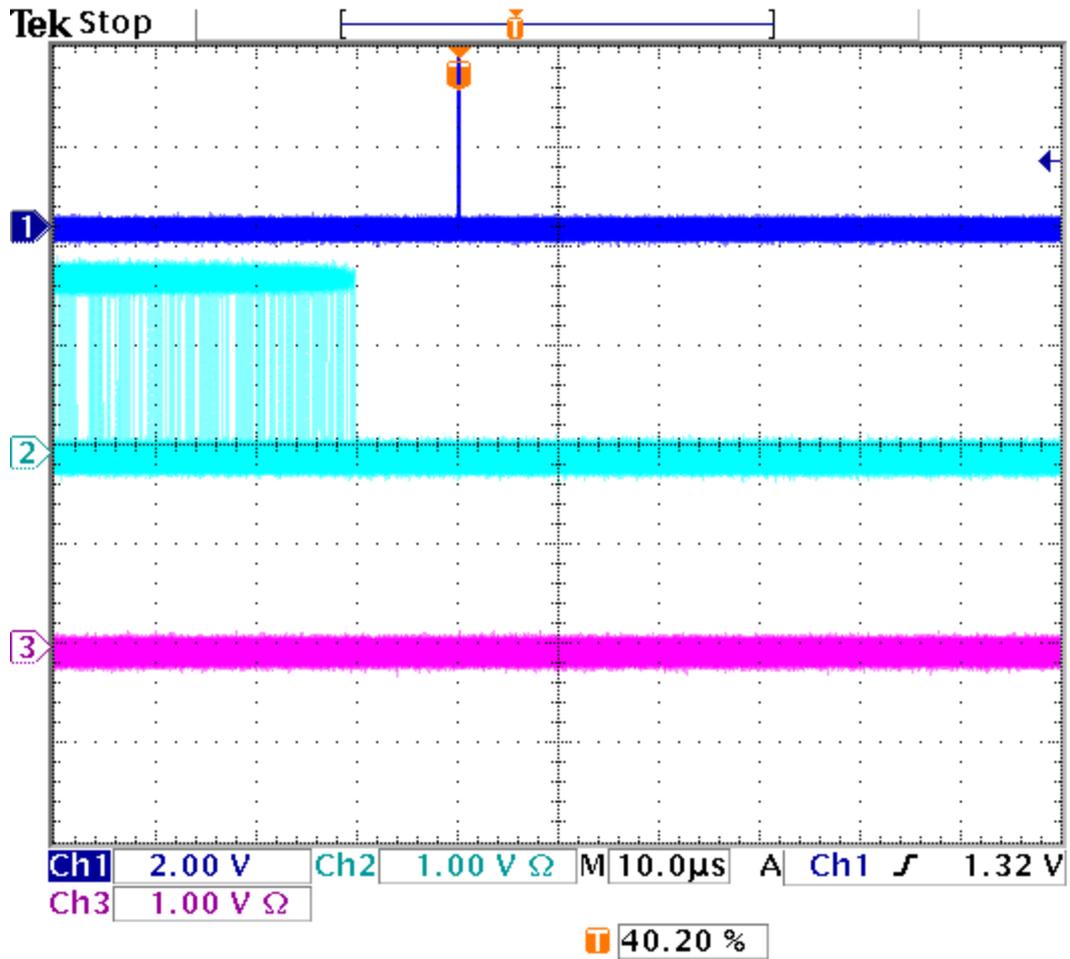
Test conditions

- Modified version of Ben's DS10 daqman code (mftest_v1-1)
- V1720B and V1720 ADCs set to 10 buffers
- Acquisition window set to 300 μ S
- External 50 MHz quartz clock source
- External Run Enable signal
- V1495 trigger logic preventing trigger overlap
- Variable trigger rate from HP 8110A pulser (1 Hz - 1 MHz)

Trigger signal (Ch1) and Memory Full signals (Ch2 & Ch3)

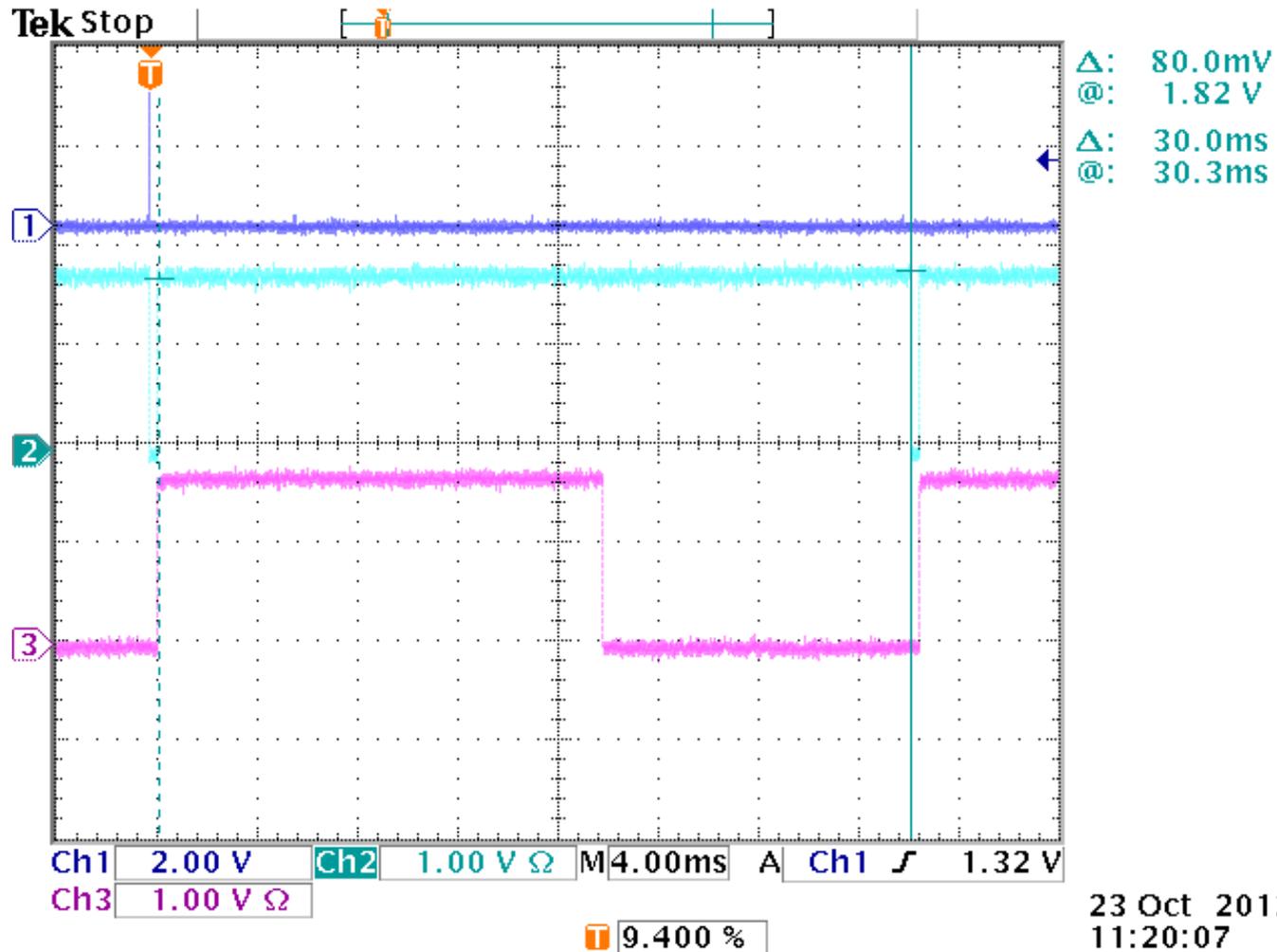


A 10 μS trigger block after MF

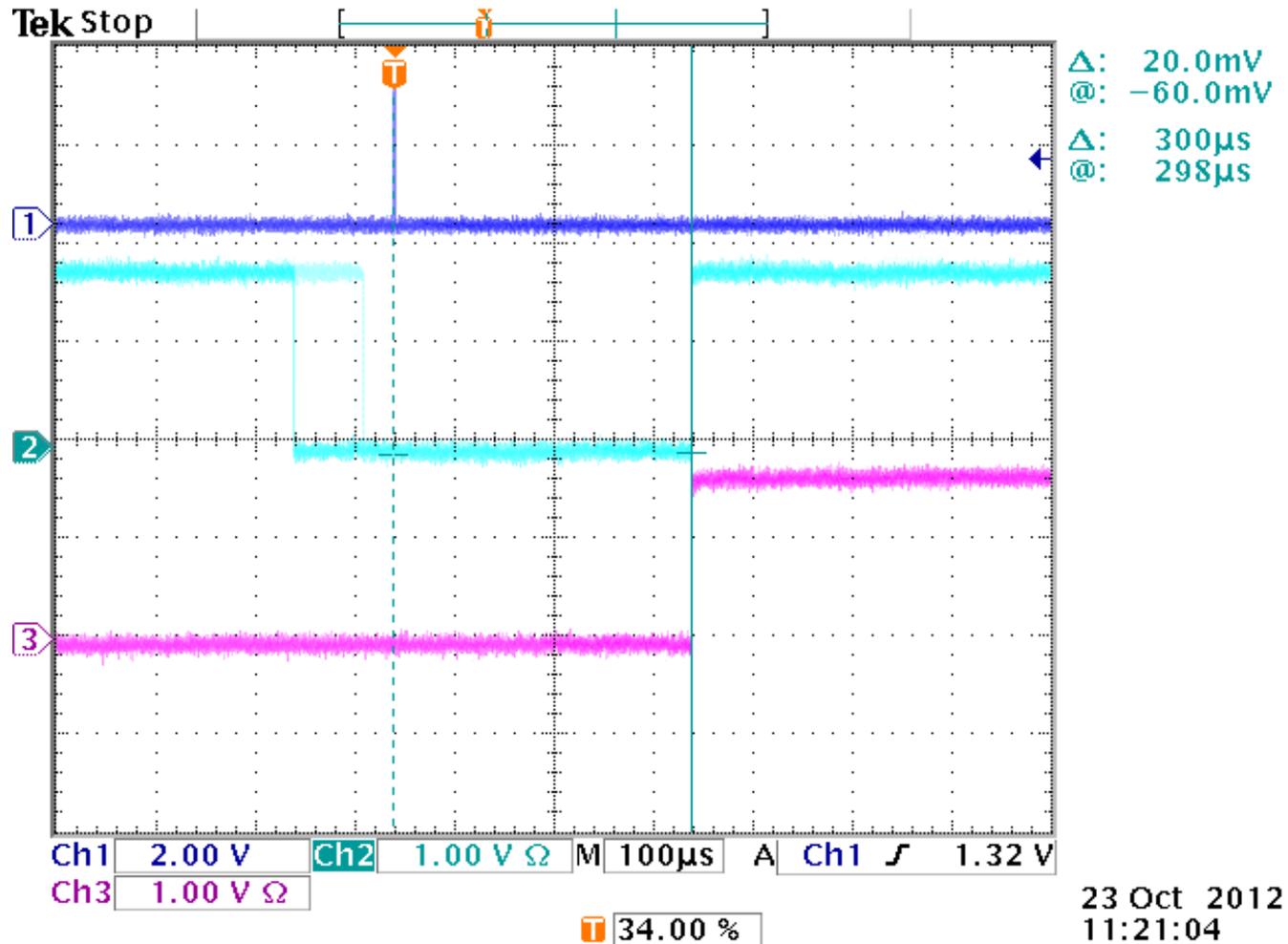


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Trigger and Memory Full signals



Trigger and Memory Full signals



Preliminary conclusions

- Memory Full signals are fully functional
- Triggers have to be blocked for at least an acquisition window interval
- Memory Full signals have to be extended by approximately 10 μ S
- Event Counter register of the V1720 is a good tool to verify event synchronization

MF extension study

- A variable one-shot fired at the falling edge of ORed Memory Full signals
- The trigger inhibit one-shot was set to 310 μs
- Error free operations observed when the duration of the variable one-shot was not less than 960 ns
- Stable operations were observed with the input trigger rate up to 1 MHz

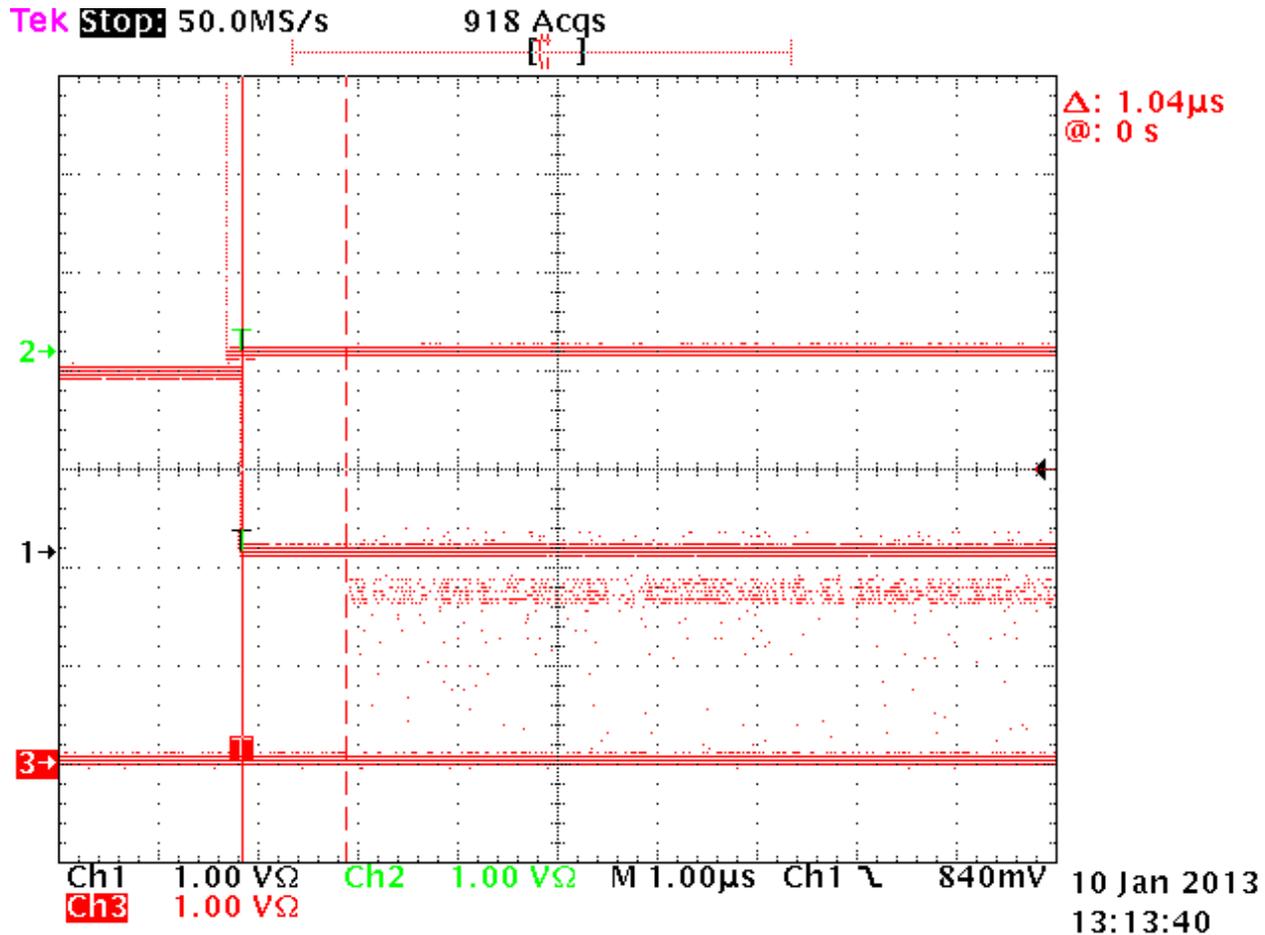
New Firmware Testing

- New firmware provided by CAEN was tested using the same setup
- The firmware allows a chain OR of the ADC Memory Full signals to be connected to the TRG OUT connector of the ADC
- This arrangement will simplify ADC cabling since only one coaxial cable needed to connect to V1495 TPC Memory Full input

MF Extension with the new firmware

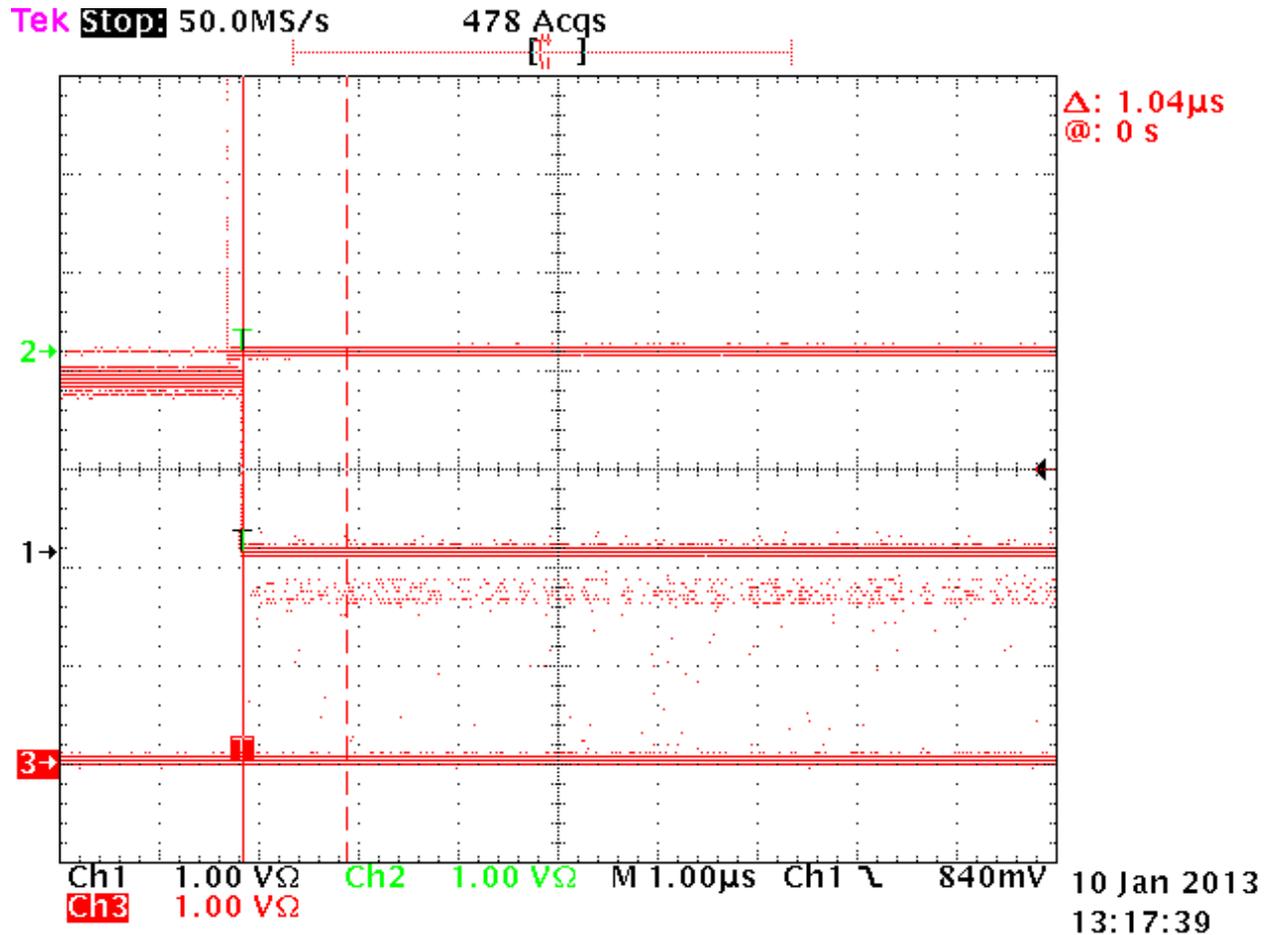
- CAEN claimed that extension of the MF signal we have reported to them is not necessary anymore with the new firmware
- The following scope pictures illustrate that it is true
- In both cases (with and without extension) the prototype DAQ system was running errorless with the input trigger rates up to 1 MHz

Extension of the MF signal for $\sim 1\mu\text{S}$



Ch1 – ORed Memory Full signals, Ch3 – V1495 trigger output

No MF signal extension



Ch1 – ORed Memory Full signals, Ch3 – V1495 trigger output

Conclusions

- Stable configuration of the Memory Full logic firmware has been tested and finalized
- Trigger inhibit for the duration of the ADC's acquisition window is required for error free operation
- New firmware allows easy combining of the Memory Full signals
- Estimated interrupt processing time is ~ 2.4 mS