

Gated trigger for the DarkSide 50 Veto System

The DAQ of the DarkSide 50 experiment includes TPC digitizers and Veto digitizers. The TPC DAQ uses CAEN v1720 modules and the Veto System uses NI PXIe-5157 modules. The main difference between two digitizers is the width of the acquisition window. For the PXIe-5157 it is 60 μ S, while for the v1720 it is 300 μ S. It is highly desirable to synchronize two types of the digitizers with the TPC trigger, so full background information is available for each TPC event. At the time of this writing there is no information available at National Instruments web site on the PXIe-5157 digitizer. It is assumed below that this digitizer behaves similarly to the CAEN v1720 in terms of event buffering and triggers overlap.

The following scheme is proposed to satisfy this synchronization requirement. The TPC trigger and 8-bit Trigger ID are transferred via optical link to the v1495 module located at the Veto System site. The v1495 logic decodes Trigger ID and places it in a FIFO memory for the readout via VME bus as a part of the TPC data stream. The output of the FIFO is also available for the Veto DAQ readout via digital I/O register (part of the PXI-6602 module). Arriving TPC trigger generates 300 μ S gate which selects only Veto triggers within this window to trigger Veto digitizers. In order to mark the beginning of the gate and provide a trigger when there is no Veto Hardware Trigger, an Extra Trigger is generated at the same time and ORed with the gated Veto triggers. The readout of the Veto System digitizers has to be driven by the interrupt generated by the TPC Trigger. For event synchronization purpose the number of triggers sent to the Veto digitizers is independently counted by v1495 and by a counter in the PXI-6602 module. Another counter in the PXI-6602 module is used to count Extra Triggers generated by the v1495. Each counter has to be reset after readout. The former counter provides the number of events to be readout for each TPC trigger. The latter counter provides verification mechanism for the busy status of the Veto DAQ. The trigger count should be always one when no busy status occurs. The busy status will occur when the Veto DAQ is still reading out the event and another TPC trigger arrives. This puts a requirement on the Veto DAQ to readout all events in the Veto digitizers before the next TPC trigger arrives. Assuming that Veto System can be read out in a few milliseconds, this requirement can be easily satisfied by limiting TPC trigger rate at the level of a few hundred hertz. Another issue can arise when Veto Hardware Trigger arrives within 60 μ S of the TPC trigger. This has to be resolved at the Veto DAQ System either by allowing overlapped triggers or disabling them. The block-diagram of the proposed scheme is shown in Figure 1.

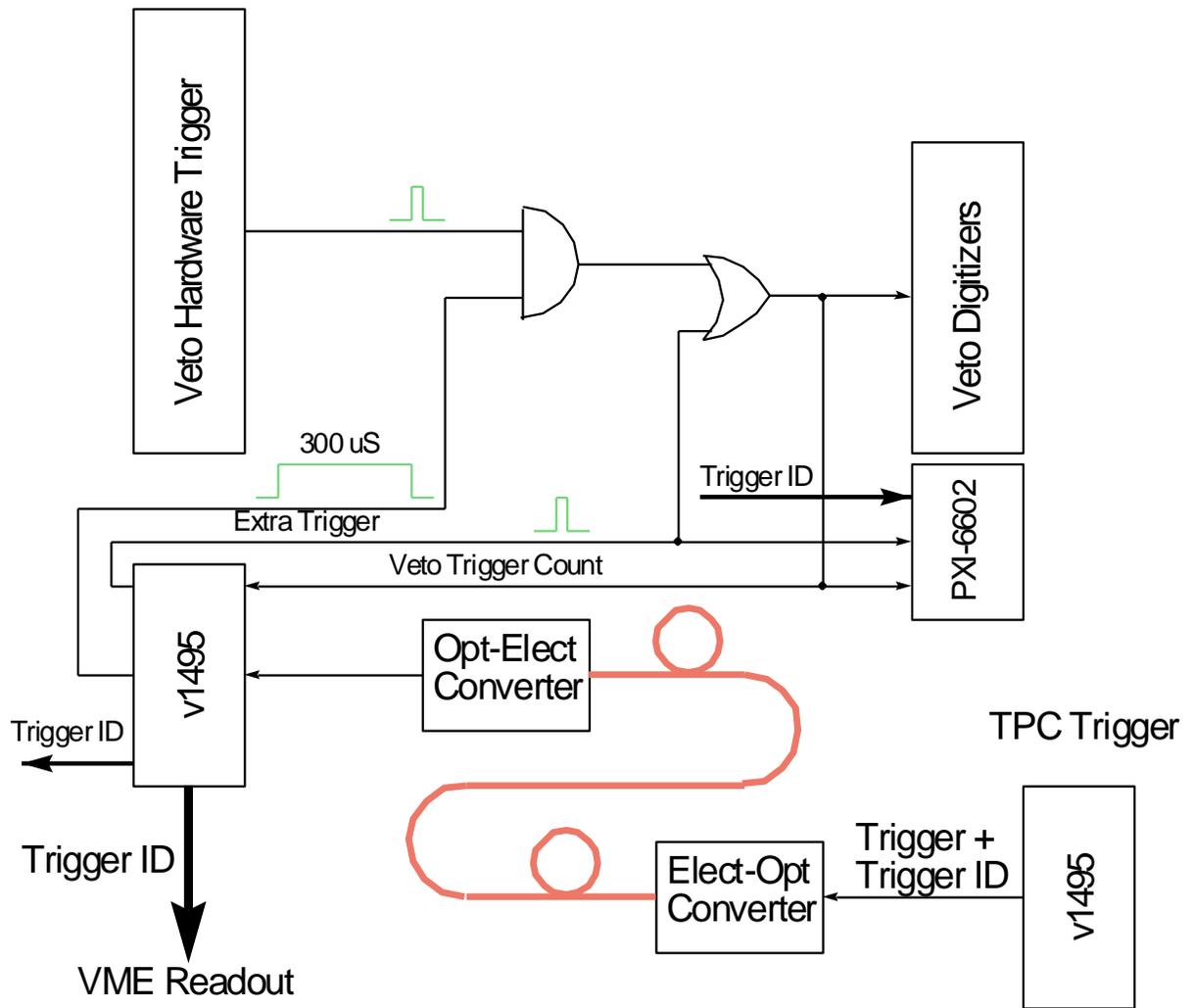


Figure 1. Block-diagram of the proposed gated trigger for the Veto System.