

## DS50 Event Synchronization

### 1. Introduction

DS50 setup will use multiple V1720 ADCs. Reading out event data from ADCs with continues trigger stream will put them in unequal status: some ADCs may be ready for the next trigger, while others may still be in Memory Full status and, therefore, reject the triggers. The proposed solution of using Memory Full LVDS signal from the V1720 I/O connector to block the triggers while any ADC is busy will work, but may present an event synchronization issue. In order to detect possible loss of the event synchronization existing features of the V1720 could be used.

### 2. Event synchronization in V1720

As designed, the V1720 provides two registers in the event data header: Trigger Time Tag and Event Counter. The Trigger Time Tag is a 32-bit 125 MHz counter latched at the arrival of the trigger. The 24-bit Event Counter can be programmed to count only accepted triggers. Having this information allows one to identify the mismatch of the events very easily. Every good event from different ADCs should have identical time tag and event count (see Figure 1). Of course, both counters have to be properly synchronized at the beginning of the run. A proper synchronization of the ADCs can be achieved in two different ways: chained signal distribution and star-like signal distribution. The latter has certain advantages and I propose to use it.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1 0 1 0				EVENT SIZE																											
BOARD-ID				RESr 0				PATTERN												CHANNEL MASK											
reserved				EVENT COUNTER																											
TRIGGER TIME TAG																															
0 0 0 0				SAMPLE [1] - CH[0]												0 0 0 0				SAMPLE [0] - CH[0]											
0 0 0 0				SAMPLE [3] - CH[0]												0 0 0 0				SAMPLE [2] - CH[0]											
0 0 0 0				SAMPLE [N-1] - CH[0]												0 0 0 0				SAMPLE [N-2] - CH[0]											
0 0 0 0				SAMPLE [1] - CH[1]												0 0 0 0				SAMPLE [0] - CH[1]											
0 0 0 0				SAMPLE [3] - CH[1]												0 0 0 0				SAMPLE [2] - CH[1]											
0 0 0 0				SAMPLE [N-1] - CH[1]												0 0 0 0				SAMPLE [N-2] - CH[1]											
0 0 0 0				SAMPLE [1] - CH[7]												0 0 0 0				SAMPLE [0] - CH[7]											
0 0 0 0				SAMPLE [3] - CH[7]												0 0 0 0				SAMPLE [2] - CH[7]											
0 0 0 0				SAMPLE [N-1] - CH[7]												0 0 0 0				SAMPLE [N-2] - CH[7]											

Figure 1. CAEN V1720 Event Organization

In this scheme Clock, Trigger and Run signals have to be distributed to all ADCs with equal delays. The 2x8-channel V976 fanout module from CAEN can be used to distribute Trigger and Run signals. For the clock distribution an LVDS fanout is needed (see Figure 2). As required by the V1720 specification, both Trigger and Run signals have to be synchronized to the ADC clock. An additional clock output from the Clock FanOut module is used to provide ADC clock to the trigger unit (V1495).

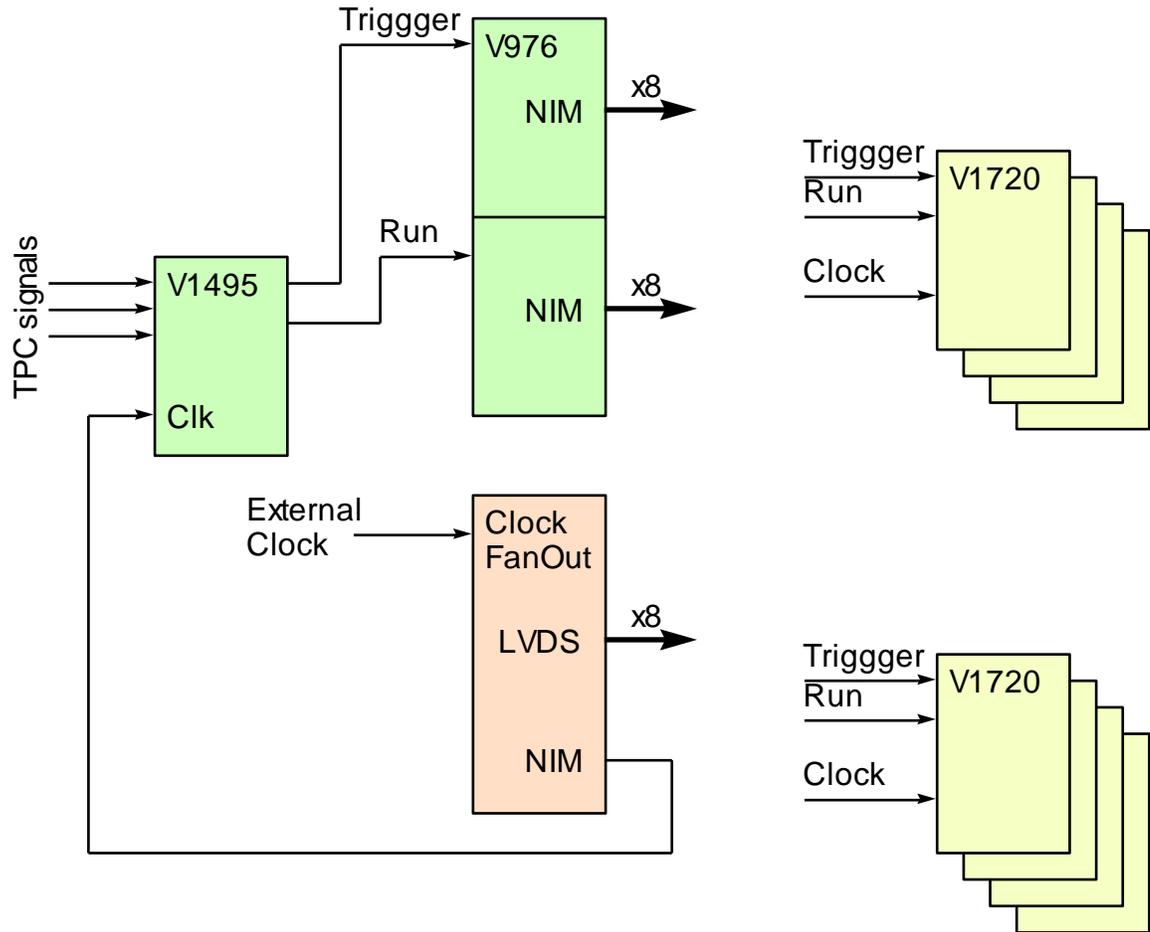


Figure 2. Proposed DS50 Star Topology Signal Distribution.

### 3. The LVDS Clock FanOut

The LVDS Clock FanOut VME module can be built by Fermilab. The following features are proposed to implement:

- Internal 50 MHz quartz oscillator
- External NIM/TTL clock input (LEMO)
- On-board switch to select the clock source (Internal/External)
- Eight LVDS clock outputs (AMP)
- Two NIM/TTL clock outputs (LEMO)
- Only +5V power used by the module from the VME connector

The estimated cost of producing *one module* (five total) is ~\$500.00. Required labor effort is approximately two (2) months (design + assembly). Detailed cost estimate can be provided if decision of producing the module is made.