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Characterization of an electronic front-end for Dark Matter related signals conditioning

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A mamma e papa

Abstract

This work is dedicated to a front-end board which works within the INFN DarkSide-50 experiment for Dark Matter search. It begins with an introduction about the basic ideas of this physics field and about the structure of the experiment. A second section covers the basic theory of the most important electronic circuits and components involved in the front-end board. Its design is then discussed in detail and a final chapter shows and comments the measurements done on the board. Since the main purpose of the front-end design - as specified later in the work - is to have a really low noise level, a brief appendix on electrical noise is provided to explain some considerations expressed in the main body of the work.

Acknowledgements

This work could not be possible without the willingness of Alessandro Razeto and the electronic division of LNGS, specially in the persons of Marco D'Incecco, George Korga and Giuseppe Bonfini. All the measurements were done at LNGS, with the help, the passion and the patience of these guys.

I want to strongly thank Marco D'Incecco, the front-end main designer, for having dedicated his time to explain to me the board functionalities and his designing tips and tricks.

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Contents

1 Introduction **10**

1.1 Structure of the experiment 11

1.2 Photomultipliers 15

1.3 Electronics 18

1.3.1 Cryogenic Amplifier 18

1.3.2 Gain stage and digitizers 18

2 Basic electronic configurations **20**

2.1 Operational Amplifier 20

2.1.1 Working principles 20

2.1.2 Configurations 23

2.1.3 Non idealities of a real operational amplifier 28

2.2 Passive filters: RLC low-pass filter 30

2.3 Digital to Analog Converter (DAC) 33

2.4 Printed Circuit Board (PCB) 37

3 The Front-End section **42**

3.1 Block Diagram 42

3.2 Amplification 46
3.3 Analog outputs: buffering and filtering 47
3.4 Digital output: threshold and discriminator 54
3.4.1 Threshold 54
3.4.2 Discriminator 62
3.5 Noise-reduction techniques 65

4 Measures 68

4.1 Amplification and fall time 68
4.2 Bandwidth 79
4.3 Noise 82
4.4 LVDS output: discriminator activation and jitter 83

5 Summarizing 90

A Noise 91

List of Figures

1.1 LAr TPC schematic structure and section. 13
1.2 TPC assembling. 14
1.3 TPC placing. 15
1.4 Structure of a photomultiplier 16
1.5 The Hamamatsu R11065 PMT. 17

2.1 Operational amplifier circuital symbol. 21
2.2 Negative feedback scheme. 23
2.3 Operational amplifier in the inverting configuration. 24
2.4 Operational amplifier in the non-inverting configuration. . . . 25
2.5 Operational amplifier in the buffer configuration. 26
2.6 Open loop function of operational amplifiers. 27
2.7 The operational amplifier transfer function. 29
2.8 The RLC series circuit. 32
2.9 The transfer function of a resonant RLC circuit. 33
2.10 DAC realized with R-$2R$ resistor ladder. 34
2.11 PCB trace over the ground plane. 39

2.12 Trace corners layouts: rounding has the best effects in avoiding reflection. 39
2.13 Crosstalk between two traces and ground plane effect. 41

3.1 Front-end top and bottom. 43
3.2 Block Diagram of the front-end section. 44
3.3 Front-end inputs and outputs. 45
3.4 The 8 front-end boards in action on the experiment. 46
3.5 The amplification section of the Front-End. 48
3.6 The buffering and filtering section of the Front-End for amplified outputs. 51
3.7 THS3061 transfer functions for $R_f = 357\ \Omega$, $560\ \Omega$ and $1000\ \Omega$. 53
3.8 The buffering and filtering section of the Front-End for the buffered output. 55
3.9 The voltage reference generation: the LM4140 and its buffering stage. 56
3.10 The MAX5116 DAC with DIP switch, for the automated control of threshold. 58
3.11 The trimmers for the manual control of threshold. 60
3.12 Threshold selection: the TS5A3160 switch and its control bit's generation. 63
3.13 Threshold buffering with a non-inverting operational amplifier. 64
3.14 Transfer function for a comparator with hysteresis. 66
3.15 The ADCMP552 discriminator and PECL to LVDS conversion. 67

4.1 The NIM crate for the front-end placement. 69

4.2 Fast output with 20 mV in input. 72
4.3 Fast output with 51 mV in input. 72
4.4 Fast output with 126 mV in input. 73
4.5 Fast output with 190mV: beginning of saturation. 73
4.6 Filtered output with 30 mV in input. 74
4.7 Filtered output with 76 mV in input. 74
4.8 Filtered output with 187 mV in input. 75
4.9 Buffered output with 77 mV in input. 75
4.10 Buffered output with 188 mV in input. 76
4.11 Buffered output with 487 mV in input. 76
4.12 Fall time of the fast output. 77
4.13 Fall time of the filtered output. 77
4.14 Fall time of the buffered output. 78
4.15 Transfer funcion of the fast output. 80
4.16 Transfer funcion of the filtered output. 81
4.17 Transfer funcion of the buffered output. 81
4.18 Noise level of the fast channel. 84
4.19 Noise spectrum of the fast channel. 84
4.20 Noise level of the filtered channel. 85
4.21 Noise spectrum of the filtered channel. 85
4.22 Noise level of the buffered channel. 86
4.23 Noise spectrum of the buffered channel. 86
4.24 Noise spectrum density of the buffered channel. 87
4.25 Noise spectrum density of the buffered channel. 87
4.26 Discriminator activation: the LVDS output. 88

4.27 Jitter standard deviation. 89

Chapter 1

Introduction

Back in 1933, Swiss astronomer Fritz Zwicky was analyzing the Doppler velocities of whole galaxies within the Coma cluster. He found that the individual galaxies within the cluster were moving so fast that they would have escaped if the cluster was held together only by the gravity of its visible mass. The phenomen was then confirmed sperimentally by American astronomer Vera Rubin in the '70s. The fact led physicists to hypotize the existence of invisible matter, meaning that it has no interaction with light: no light absorbtion, no light emission, no light reflection. That is why this matter was named *dark matter*.

Recently, within the formulation of the Supersimmetry theory in particle physics, was theorized the existence of massive particles with no electric charge (so unsensitive to electromagnetic forces and consequentially to light) that would be sensitive only to gravitational and weak interactions, called WIMPs (Weak Interaction Massive Particles). They seem to be the ideal candidate to solve the mystery of dark matter.

If they exist, WIMPs should form a cold thermal relic gas, which could be detected via elastic collisions with nuclei of ordinary matter. This is expected to be a rare event, because of the weak coupling between WIMPs and ordinary matter.

Evidence for such WIMPs may come from experiments at the Large Hadron Collider at CERN or from sensitive astronomical instruments detecting radiation produced by WIMP-WIMP annihilations in galaxy halos. The orbital motion of the WIMPs in the dark matter halo pervading the galaxy should also result in WIMP-nucleus collisions of sufficient energy to be detected directly by sensitive laboratory apparatus. The detection of these WIMPs is based on the capability of measuring the recoils of target nuclei with kinetic energy in the range of 10-100 keV. Since natural radioactivity (such as beta or gamma, or neutrons) causes background right in this energy range, some accurate techniques has to be applied to reject it. This is what is running in the DarkSide-50 experiment, prepared in the Gran Sasso laboratories (LNGS).

1.1 Structure of the experiment

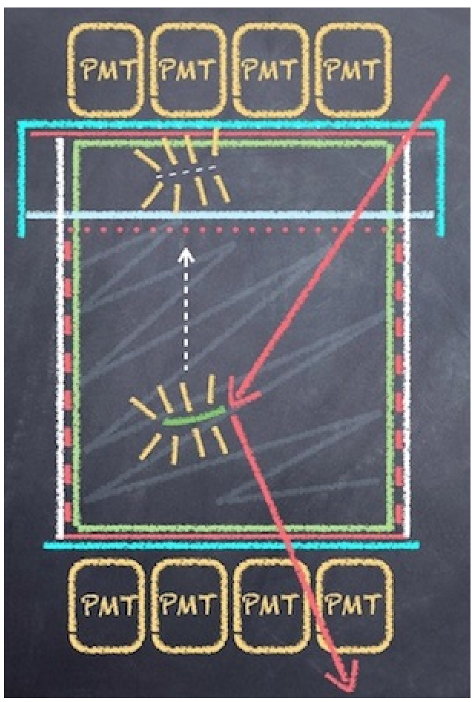
First of all, the active medium for detection of dark matter WIMPs is liquid Argon (LAr), a cryogenic material with excellent scintillation and ionization properties. If WIMPs exist they are expected to collide with nuclei and produce recoil atoms with kinetic energies up to about 100 keV. The recoil atoms produce a short track of ionized and metastable excited argon atoms. After the initial ionizing event, a sequence of reactions occurs that involves recombination of electron-ion pairs and ends with formation of short-lived excited diatomic argon "molecule". These decay with emission of the characteristic 128-nm scintillation light. Free ionization electrons that have not recombined also remain. Here is where the choice of liquid Argon as a target comes from.

These events can be detected by observing both the prompt scintillation light and the free ionization electrons. There are key differences in the response of LAr to low density-ionization events, such as β or γ interactions (electron recoils) from residual radioactivity in detector materials, compared to the sought-after heavily-ionizing nuclear recoil atom events. Low density-ionization results in less recombination and so more free electrons than a nuclear recoil of the same total energy. The difference in ionization density also produces a relevant difference in the time profile of the scintillation light from low to high ionization-density events: the scintillation time profile (a pulse shape) depends on the nature of the ionizing particle, providing particles discrimination that can be used to suppress background. These elements provide a powerful background rejection that is unique to Argon.

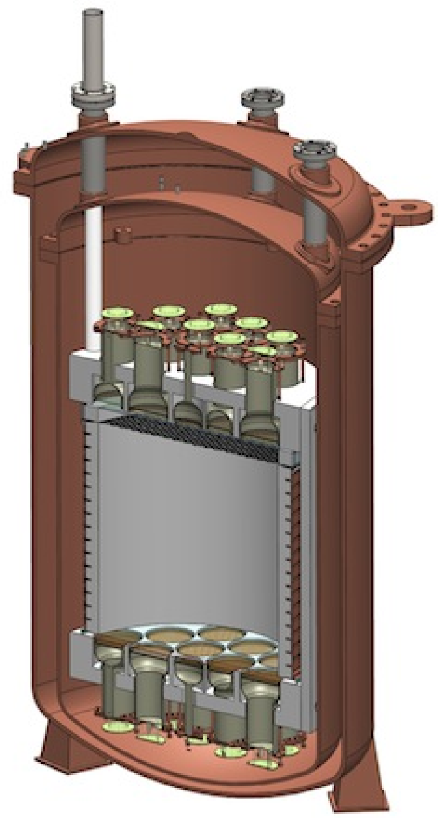
As for what concerns nuclear recoils from the scattering of cosmogenic neutrons and radiogenic neutrons from residual radioactivity in detector components, these events will be measured and rejected using nested shields of borated liquid-scintillator surrounding the Argon detector as a neutron veto and a water Cherenkov detector as a muon veto. This in addition to the fact that the whole experiment is located in deep underground to reduce cosmic ray muons background before the vetos. To exploit these powerful background suppression characteristics requires a two-phase liquid Argon *Time*

Projection Chamber (LAr TPC) made of low radioactivity components and with efficient collection of both scintillation light and ionization charge.

The LAr TPC design is schematically shown in Figure 1.1.



(a) Schematic structure



(b) Section

Figure 1.1: LAr TPC schematic structure and section.

The inner detector contains the active liquid Argon volume. Arrays of photodetectors view the active volume from the top and the bottom. The inner surfaces of the active volume are coated with a vacuum-evaporated thin film of tetra-phenylbutadiene wavelength shifter, which shifts the 128 nm UV primary scintillation (S_1 signal) into the visible for detection.

To detect the ionization, an electric field is produced to drift the ionization electrons up to the surface of the liquid. There, an electric field of 3 kV/cm extracts the electrons into Argon in gas phase, where they produce secondary scintillation photons by a process called *electroluminescence*. The resulting secondary photons (S_2 signal) are detected by the photodetector array as a delayed phenomenon related to the primary scintillation S_1.

The LAr TPC allows events to be accurately localized in three dimensions. The delay time between S_1 and S_2 defines the vertical position of each event to millimeter precision. The distribution of light over the top photo detector array gives the horizontal position to centimeter precision.

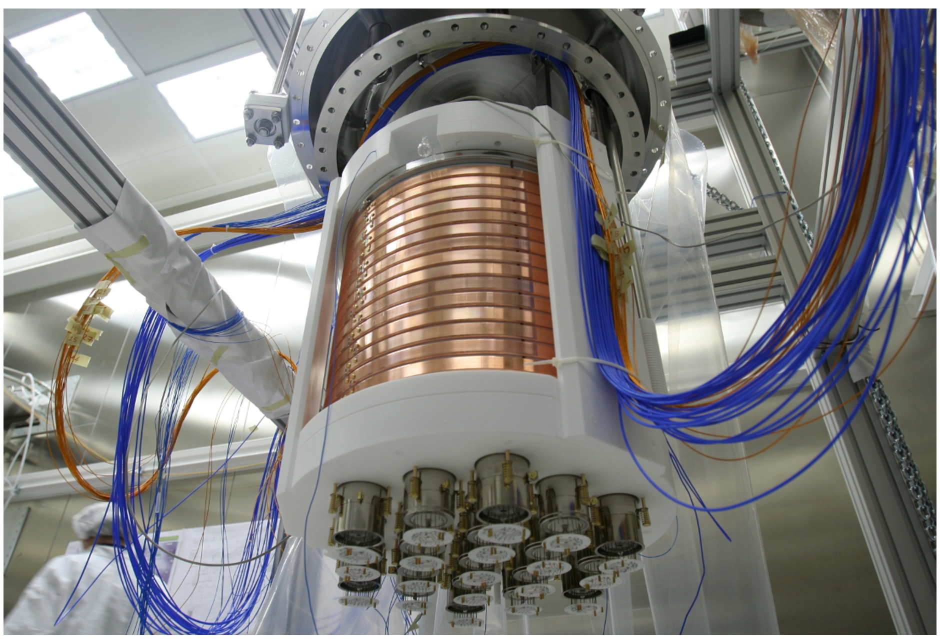


Figure 1.2: TPC assembling.

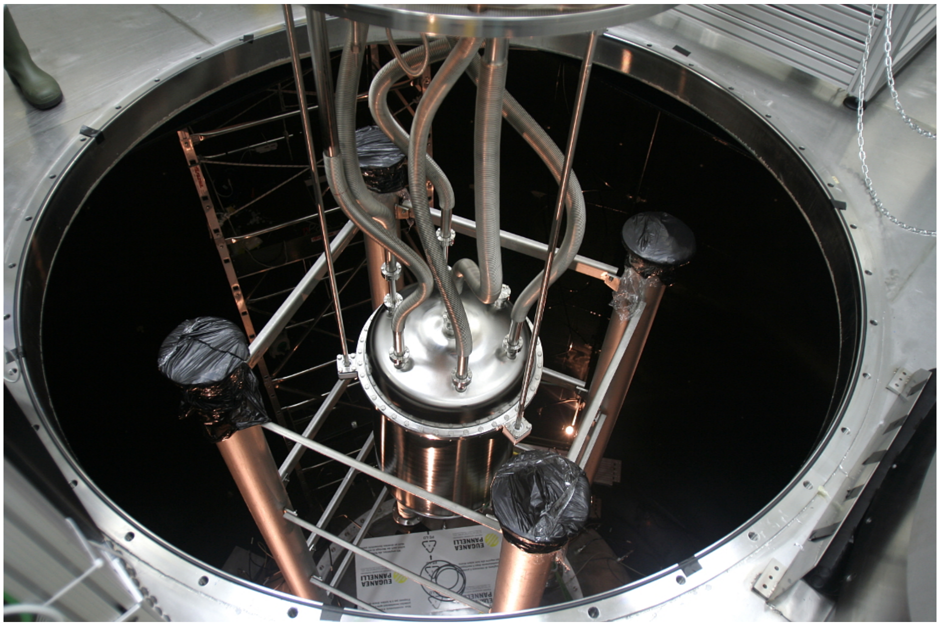


Figure 1.3: TPC placing.

1.2 Photomultipliers

The first detection step is made of photomultipliers: these devices can convert a light input into a current output.

Photomultipliers are constructed from a glass envelope with a high vacuum inside, which houses a photocathode, several dynodes, and an anode (see Figure 1.4). Incident photons strike the photocathode material, which is present as a thin deposit on the entry window of the device, with electrons being produced as a consequence of the photoelectric effect. These electrons are directed by the focusing electrode toward the electron multiplier, where electrons are multiplied by the process of secondary emission.

The electron multiplier consists of a number of electrodes called dynodes. Each dynode is held at a more positive voltage, by $\simeq$100 Volts, than the

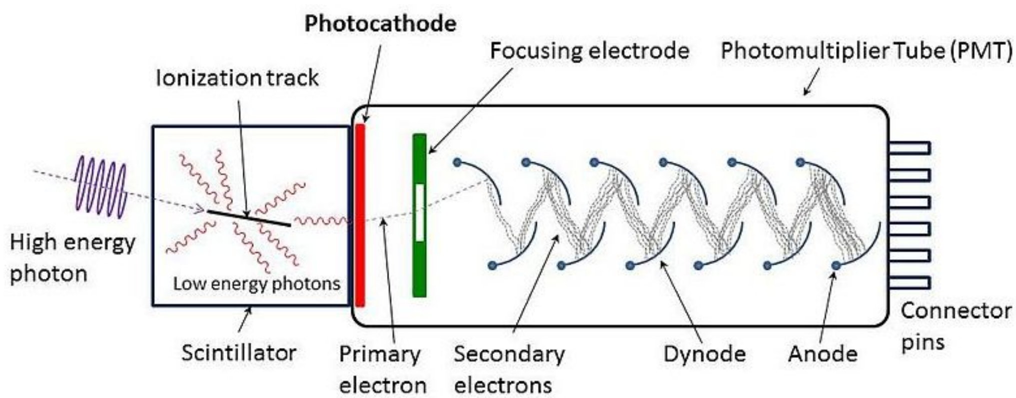


Figure 1.4: Structure of a photomultiplier

previous one. A primary electron (called *photoelectron*) leaves the photocathode with the energy of the incoming photon, minus the work function of the photocathode. As a group of primary electrons, created by the arrival of a group of initial photons, moves toward the first dynode they are accelerated by the electric field. They each arrive with $\simeq$100 eV kinetic energy imparted by the potential difference. Upon striking the first dynode, more low energy electrons are emitted, and these electrons in turn are accelerated toward the second dynode and so on for each following dynode. This large number of electrons reaching the last stage, called the anode, results in a sharp current pulse that is easily detectable.

Photomultiplier tubes typically utilize 1000 V to 2000 V to accelerate electrons within the chain of dynodes. The most negative voltage is connected to the cathode, and the most positive voltage is connected to the anode. Negative high-voltage supplies (with the positive terminal grounded) are preferred, because this configuration enables the photocurrent to be measured at the low voltage side of the circuit for amplification by subsequent electronic circuits operating at low voltage. Voltages are distributed to the dynodes by a voltage divider.

The baseline for the LAr-TPC PMTs of DarkSide-50 is the 3” ultra-low background Hamamatsu R11065.

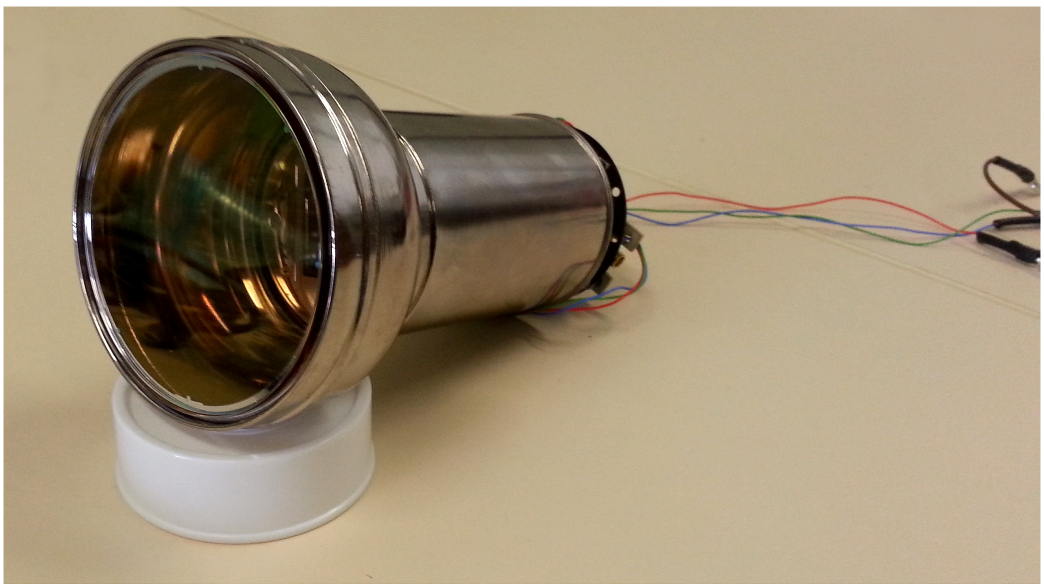


Figure 1.5: The Hamamatsu R11065 PMT.

This photocathode operates down to LAr temperature with high quantum efficiency, and is constructed of radio-pure materials. A problem with these devices is their emission of light. Was found evidence of light emission by the R11065 PMT in action at cryogenic temperature: light emission occurred above a bias voltage of 1500 V. To minimise this problem, DarkSide-50 is using PMTs with low-radioactivity cryogenic preamplifiers on their bases. The cryogenic preamplifiers allowed to reduce the PMT bias voltage to 1100 V, moving the gain from detector to electronics.

1.3 Electronics

A powerful feature of LAr as a medium for WIMP detection is the ability to suppress electron and γ background using the time profile of the scintillation signal following an energy deposition in the liquid. In order to exploit the information from the pulse shape to maximum effect, the scintillation signals detected by the TPC PMTs must be acquired with high accuracy: this is the most critical design requirement for the electronics and data acquisition chain. This requirement affects - as said before - the design of the PMT base and cold preamplifiers, and also of the analog to digital conversion.

1.3.1 Cryogenic Amplifier

Cryogenic amplifiers allow the PMTs to be operated at reduced gain. At the same time, the anode parasitic capacitance can be used to reduce signal bandwidth with no loss of accuracy. This relaxes requirements for the cables and the digitizers.

1.3.2 Gain stage and digitizers

The input to each channel of the front-end consists of the signal from the cryogenic amplifier. The digitizer *front-end* provides a bandwidth filtering and amplifies the signal, which is then sent to two Analog to Digital Converter

(ADC) branches. The first ADC branch has 10x gain and is used for recording small signals with optimal resolution. It works at 250 MSps with 12-bit resolution, required to provide the time resolution and dynamic range needed for the primary scintillation and secondary proportional signals. The second ADC branch has a 1x gain, to capture larger amplitude signals, typically from S2, without saturation. It works at 100MSps.

Each front-end board is mounted within a NIM module, a standard for particle physics. A total of 8 boards are working in DarkSide-50, and each board contains 5 channels and therefore follows 5 PMTs.

Chapter 2

Basic electronic configurations

In this chapter we'll go through the basic configurations of the main electronic devices used in the digitizer's Front-End. For each device, there will be a short introduction about its operation and features.

2.1 Operational Amplifier

2.1.1 Working principles

An ideal operational amplifier is an integrated circuit with:

- infinite voltage gain;
- infinite input impedance and null output impedance;
- infinite working bandwidth

In the physical reality, though, it provides a high (but not infinite) gain and input impedance (so that there will always be an input noise current), and a low output impedance. Other non-idealities will be examined later.

In the input section there are two pins for two signals: they are called "non-inverting" and "inverting" inputs (later in this chapter will be explained why these names were chosen.) and respectively indicated as v_+ and v_-. On the scheme, they're visualized with the signs + and − inside the operational amplifier circuital symbol (Fig. 2.1).

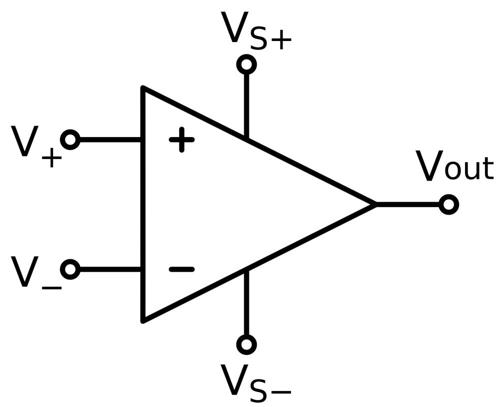


Figure 2.1: Operational amplifier circuital symbol.

The signal amplified by the operational amplifier is the difference between the non-inverting and the inverting inputs. This is practically the same principle of a differential amplifier: in fact, the input stage of an operational amplifier is always made of a differential amplifier.

Indicating as A_{OL} the "Open Loop" gain (meaning with "open loop" that nothing is being connected between output and inputs), we have:

$$v_{out} = A_{OL}(v_+ - v_-) \tag{2.1}$$

Since it is made of transistors, the operational amplifier needs a power supply. In most applications, the power supplying voltage field is dual: this means that two equal and opposite voltage references are needed. The voltage references are indicated with V_{S+} and V_{S-} in Fig. 2.1.

The most simple way to use an operational amplifier is to connect the inverting input to ground and sending a signal v_s to the non-inverting input. This would lead to:

$$v_{out} = A_{OL}(v_+ - v_-) = A_{OL} \cdot v_s \tag{2.2}$$

The problem is that the function stops very soon being linear because the dynamic range of the device is limited by the voltage supply references.

This happens even at really low input levels, because of the incredibly high gain A_{OL}; therefore the behavior of the operational amplifier examined here could be used to create a discriminator (we'll see this later in this chapter), but it's kind of useless as an amplifier.

A more useful linear amplification can be obtained by availing of *feedback* theory: we'll talk about its general features to understand how it can stabilize amplification gain. In a generic system, a feedback occurs when a part of the output is taken back to the input: this is described by the word *feedback* because the input is feed back from the output. When we subtract the portion of output from the input, we obtain a negative feedback.

Indicating with β the amplification of the feedback network and, from now on, with A instead of A_{OL} the open loop amplification:

$$\beta = \frac{v_f}{v_{out}} \tag{2.3}$$

and

$$v_{out} = A(v_s - \beta v_{out}) \tag{2.4}$$

We can now extract the expression of the amplification of the whole block, A_f:

$$A_f = \frac{v_{out}}{v_s} = \frac{A}{1 + \beta A} \tag{2.5}$$

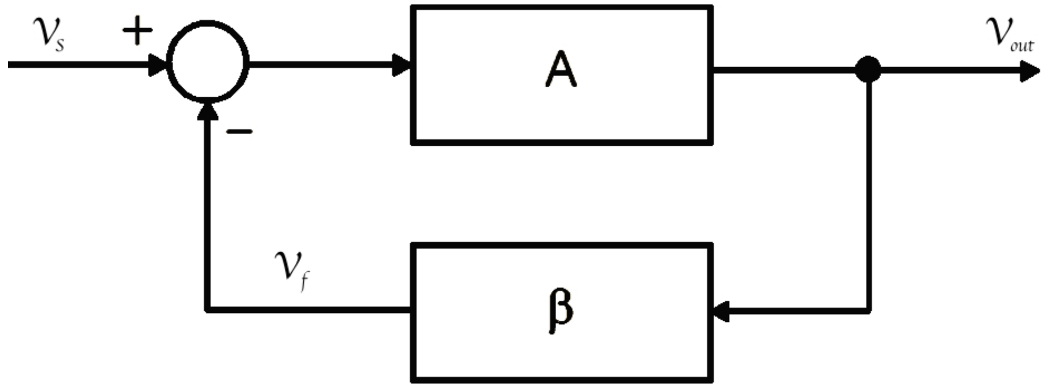


Figure 2.2: Negative feedback scheme.

The system is very stable: any unwanted variation of A is compensated by the feedback network. Also, when A is very high (as it happens with operational amplifiers), notice that

$$A_f = \frac{A}{1 + \beta A} \approx \frac{1}{\beta} \tag{2.6}$$

meaning that the amplification of the whole system does not depend anymore on A, but only on β.

2.1.2 Configurations

Now we are ready to analyze a closed-loop circuit with an ideal operational amplifier. Remembering its features, there are two fundamental effects to be considered:

- The input section draws no current because of the infinite input impedance
- The voltage difference between the inputs is zero because of the infinite gain

The two inputs are therefore at the same potential or, as commonly said, in *virtual shortcut* (or virtual ground, when one of the inputs is connected to ground).

Inverting Amplifier

In the *inverting* configuration the input signal goes into the inverting input and the non-inverting one is connected to ground. As we can see in Fig. 2.3, the feedback network is made of two resistors R_1 and R_2: R_2 takes the output back to the inverting input, realizing the negative feedback.

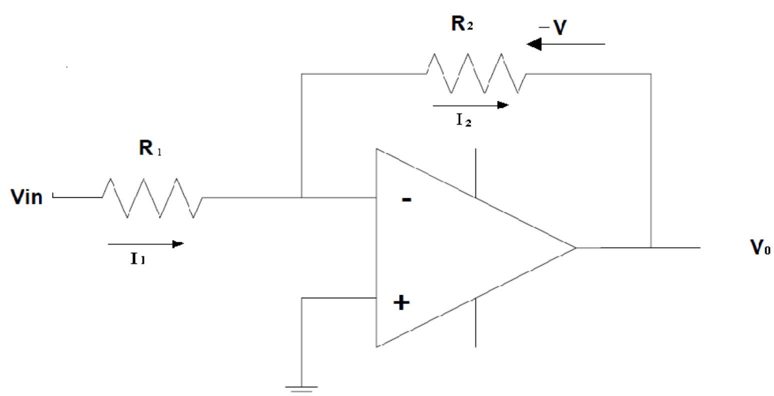


Figure 2.3: Operational amplifier in the inverting configuration.

Thanks to the virtual shortcut, v_- is at the same potential of v_+ that is connected to ground. Then, since the operational amplifier has got an infinite input impedance, the current in both R_1 and R_2 is the same. In conclusion:

$$\begin{cases} v_{out} = -iR_2 \\ v_{in} = iR_1 \end{cases} \tag{2.7}$$

obtaining for the amplification

$$A_f = \frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1} \tag{2.8}$$

Notice: this result confirms that the amplification in a counter-reacted system depends only on the feedback network.

Non-Inverting Amplifier

For the *non-inverting* configuration the skeleton of the circuit is similar to the inverting one. The feedback network is still made of two resistors R_1 and R_2 with R_2 realizing the feedback, but the input signal goes into the non-inverting input. Availing of the already discussed features of the operational

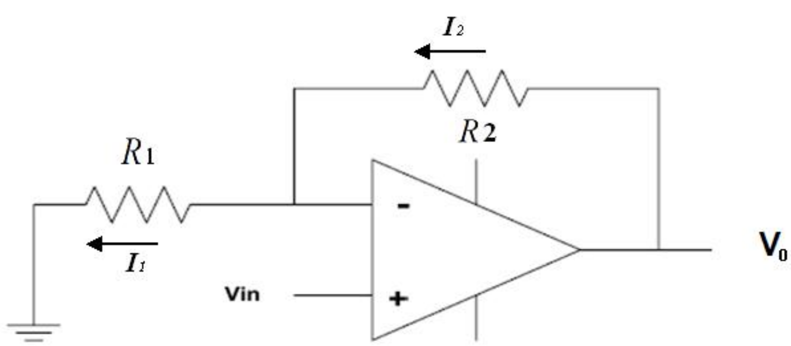


Figure 2.4: Operational amplifier in the non-inverting configuration.

amplifier, we can relate v_- to v_{out} using the relation of the voltage divider

$$v_- = \frac{R_1}{R_1 + R_2} v_{out} \tag{2.9}$$

and since $v_- = v_{in}$ we can obtain the amplification

$$A_f = \frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \tag{2.10}$$

Buffer

A *voltage buffer amplifier* is used to transfer a voltage from a first circuit, having a high output impedance level, to a second circuit with a low input impedance level. The buffer circuit provides a low output impedance, increasing the output drive capability: we can say that a buffer acts as a current amplifier. If the voltage is transferred unchanged, a *unity gain* buffer is made. The interposed buffer amplifier prevents therefore the second circuit from loading the first circuit unacceptably and interfering with its desired operation. In the ideal voltage buffer, the input resistance is infinite and the output resistance is zero.

The operational amplifier can be used as a voltage buffer amplifier with unity gain. The input signal goes to the non-inverting input, so this is a

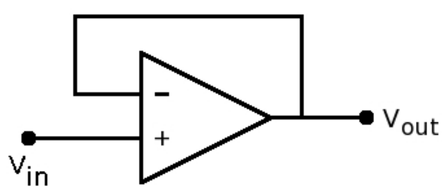


Figure 2.5: Operational amplifier in the buffer configuration.

particular case of the non-inverting configuration with $R_1 = \infty$ and $R_2 = 0$.

Looking at Fig. 2.5, it can be easily understood that

$$v_{out} = v_{in} \tag{2.11}$$

since $v_- = v_{in}$ for the virtual shortcut. The use of buffers is strongly recommended for the handling of high frequency signals and for the distribution of signals through transmission lines or on PCBs.

Discriminator

A *voltage discriminator* is a device that compares two voltages and outputs a digital signal indicating which is larger: it has two analog inputs and one digital output. This is exactly what an operational amplifier in open loop does: when the non-inverting input v_+ is at a higher voltage than the inverting input v_-, the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output, that is the upper supply voltage. When the non-inverting input v_+ drops below the inverting input v_-, the output saturates at the most negative voltage it can output, the lower supply voltage. Mathematically this is described by 2.2.

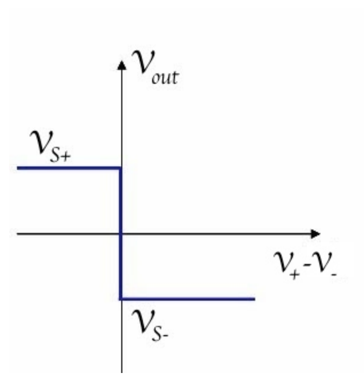


Figure 2.6: Open loop function of operational amplifiers.

2.1.3 Non idealities of a real operational amplifier

The real operational amplifiers always deviate from the ideal ones, whose concept was useful for our purpose of a general analysis. Now will be covered the most important non idealities which show up when working with such components.

Finite Bandwidth

The useful bandwidth of a system is the range of frequency in which it works without distorting the input signal. A real operational amplifier's open-loop gain is very high (and equals to A) when working with DC signals, but starts to decrease while increasing the input signal's frequency, f, ending up in causing distorsion. It is therefore a function of the frequency, that is commonly known as *transfer function*[1]. More in detail it can be modeled through the following complex transfer function:

$$A(\omega) = \frac{A}{1 + j\frac{\omega}{\omega_0}}$$

where ω is the angular velocity: $\omega = 2\pi f$, so that the previous can be written as:

$$A(f) = \frac{A}{1 + j\frac{f}{f_0}} \tag{2.12}$$

where A is the DC gain of the amplifier and f_0 is called *cut-off* frequency and it is determined by the internal construction of the amplifier. A graphical example of a transfer function like the 2.12 is reported in Fig. 2.7, where the gain is expressed in decibels (dB). About the cut-off frequency f_0, studying

[1] A more precise definition of a transfer function sees it as the relation of output and input of a system in the frequency domain.

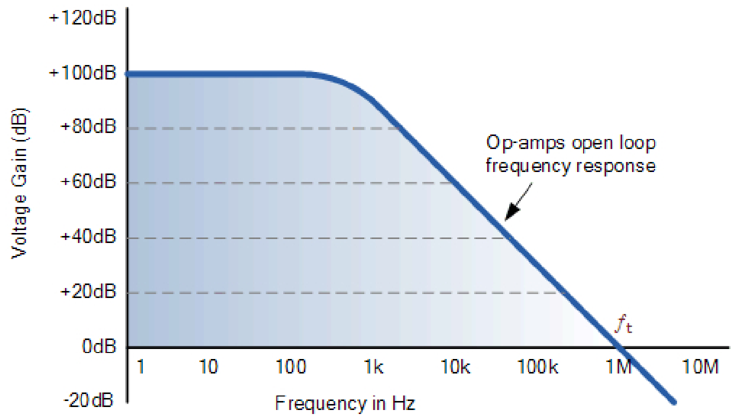


Figure 2.7: The operational amplifier transfer function.

the module of $A(f)$ it is easy to find out that for $f = f_0$

$$|A(f_0)| = |\frac{A}{1+j}| = \frac{A}{\sqrt{2}} \tag{2.13}$$

that in dB equals to a drop of 3dB. If the input signal's frequency goes higher than f_0 it will become very attenuated[2], resulting in a distorted output signal. The useful bandwidth of an operational amplifier goes therefore from 0 Hz to f_0.

This behaviour is intentionally designed by manufacturers because operational amplifiers are made of many active components, and each of them has its own cut-off frequency. Without a controlled transfer function, the amplifier's frequency response would be different from device to device even in the same family of models. The control is usually obtained with a capacitor suitably placed, but we will not go into detail for this. It is important though to specify that each operational amplifier is characterized by a constant parameter called *gain-bandwidth product* GBW, defined as the product

[2] A system which stops the frequencies above a certain one is called *low-pass filter*.

of bandwidth and closed loop gain:

$$GBW = \text{Bandwidth[Hz]} \cdot \text{Open Loop Gain}$$

a constant number expressed in Hz. This means that once chosen the gain, each operational amplifier will work with a closed loop bandwidth determined by its GBW following the relation:

$$\text{Closed Loop Bandwidth[Hz]} = \frac{GBW[Hz]}{\text{Closed Loop Gain}} \tag{2.14}$$

The bandwidth decreases as the closed loop gain increases.

Input non-null offset voltage

The *input offset voltage* V_{os} is a parameter defining the differential DC voltage required between the inputs of the operational amplifier to make the output zero.

An ideal operational amplifier amplifies the differential input, and if it is 0 V the output should be 0 V. However, due to manufacturing process, the output is zero at a non-zero value of differential input, called input offset voltage.

2.2 Passive filters: RLC low-pass filter

Electronic filters are circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal, to enhance wanted ones, or both. In this section we will go through a kind of *passive filter*. Passive filters, based on combinations of resistors, inductors and capacitors, are so-called because they do not depend upon an external power supply and they do not contain active components such as transistors.

Inductors block high-frequency signals and conduct low-frequency signals, while capacitors do the reverse. A filter in which the signal passes through an inductor, or in which a capacitor provides a path to ground, presents less attenuation to low-frequency signals than high-frequency signals and is therefore a *low-pass filter*. If the signal passes through a capacitor, or has a path to ground through an inductor, then the filter presents less attenuation to high-frequency signals than low-frequency signals and therefore is a *high-pass filter*. Resistors on their own have no frequency-selective properties, but are added to inductors and capacitors to determine the time-constants of the circuit, and therefore the frequencies to which it responds. For our purpose we will limit the analysis to a RLC filter.

RLC filter

The RLC circuit is made of a resistor R, a capacitor C and an inductor L. These components can be set both in series or parallel, but in this section we will study only the series configuration with the output on the capacitor. An RLC circuit is a resonant one: at a certain frequency f_0 of voltage and current the impedance is the minimum possible, and equals to the resistance R. The voltage output on the capacitor comes from Ohm's relation. In Laplace's domain all the parameters are in general complex numbers, so they will be indicated with a dot on their reference letter.

$$\dot{V}_C = \dot{Z}_C \dot{I}$$

where

$$\dot{Z}_C = \frac{1}{j\omega C}$$

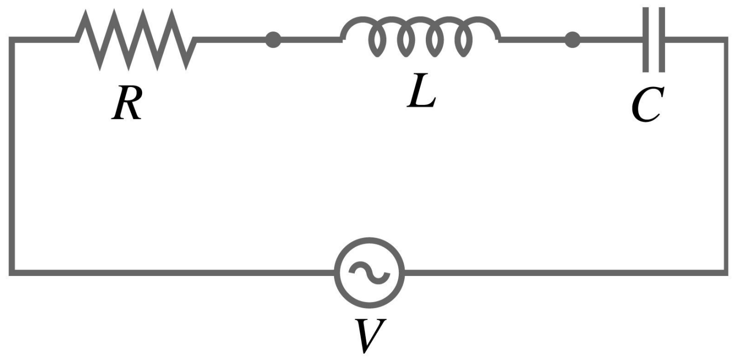


Figure 2.8: The RLC series circuit.

is the complex impedance of the capacitor C, and

$$\dot{I} = \frac{\dot{V_{IN}}}{\dot{Z_{tot}}} = \frac{\dot{V_{IN}}}{R + j\omega L + \frac{1}{j\omega C}} = \frac{\dot{V_{IN}}}{R + j(\omega L - \frac{1}{\omega C})}$$

is the current in the circuit. Notice that, expressing the module of $\dot{Z_{tot}}$ as

$$Z_{tot} = |\dot{Z_{tot}}| = \sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}$$

it is minimum when $(\omega L - \frac{1}{\omega C})^2 = 0$. Resolving for ω we have:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.15}$$

that is the *resonance angular velocity*. The *resonance frequency* is therefore

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.16}$$

We can now obtain the transfer function of the circuit, that is the relation of its output and input in the frequency domain:

$$\frac{\dot{V_C}}{\dot{V_{IN}}} = \frac{\dot{Z_C}\dot{I}}{\dot{V_{IN}}} = \frac{\dot{Z_C}}{\dot{Z_{tot}}} = \frac{\frac{1}{j\omega C}}{R + j(\omega L - \frac{1}{\omega C})} \tag{2.17}$$

whose graphic is reported in Fig. 2.9. It's easy to see that it is a low-pass transfer function, and we can demonstrate it by calculating the limit of 2.17 at low and high frequencies.

At low frequencies:

$$\lim_{\omega \to 0} \frac{\frac{1}{j\omega C}}{R + j(\omega L - \frac{1}{\omega C})} = 1 \tag{2.18}$$

so the output signal is exactly the input one, with no alterations. At high frequencies:

$$\lim_{\omega \to + \inf} \frac{\frac{1}{j\omega C}}{R + j(\omega L - \frac{1}{\omega C})} = 0 \tag{2.19}$$

so the input signal is eliminated when its frequency f is high. Practically, this happens when $f > f_0$, so that the resonance frequency can be considered as the cut-off frequency of the system.

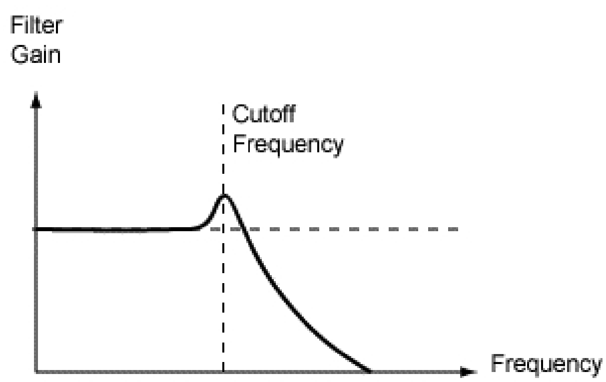


Figure 2.9: The transfer function of a resonant RLC circuit.

2.3 Digital to Analog Converter (DAC)

A *digital to analog converter* (DAC) is a function that converts digital data (usually binary) into an analog signal. Each input word is converted into a precise analog voltage.

The most common way to make a DAC is using a R-$2R$ *resistor ladder*: in Fig. 2.10 is reported a 4-bit configuration. The shown operational amplifier works mainly as a current to voltage converter, as explained in the following lines. The circuit is based only on resistors whose value is R or $2R$. Each

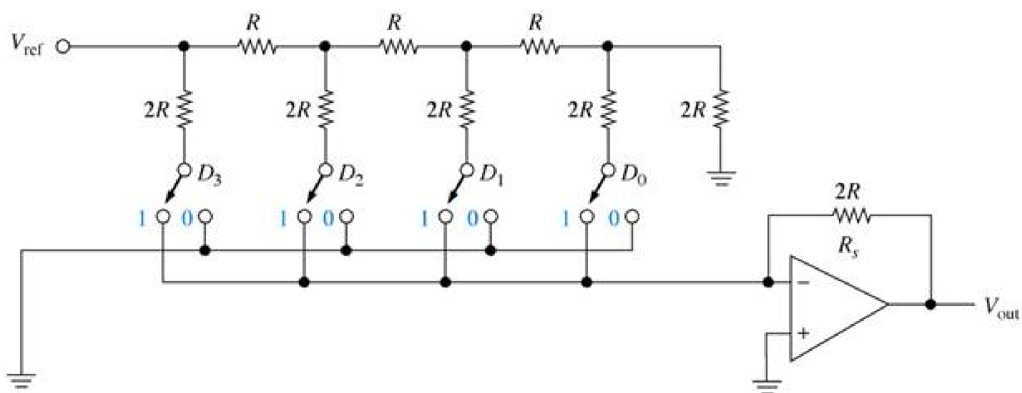


Figure 2.10: DAC realized with R-$2R$ resistor ladder.

single bit of the input word controls a switch, indicated with D_i: if it is at logic 1, the switch connects the $2R$ resistor to the inverting input of the operational amplifier. Otherwise, if it is at logic 0, the resistor is connected to ground. The Least Significant Bit (LSB) controls D_0, the Most Significant Bit (MSB) controls D_3.

This configuration allows the voltage generator to see the same equivalent resistance no matter what the switches connection is: thanks to the virtual shortcut, in fact, each $2R$ resistor is connected between V_{ref} and 0 V (ground).

We will analyze this particular case of a 4-bit DAC and then generalize the result to an N-bit DAC. Numbering the nodes from 0 to 3 starting from the extreme right, at node 0 the parallel of the two $2R$ resistors is equivalent to a R resistor. This one is in series with a R resistor, giving an equivalent $2R$ resistor in parallel with the following $2R$ resistor, obtaining an equivalent R resistor. Reasoning in the same terms till the last node, in conclusion the generator sees an equivalent R resistor that draws a constant I current:

$$I = \frac{V_{ref}}{R} \tag{2.20}$$

The equivalent resistance seen from each node is $2R$. This means that at each node the current splits in two equal currents, each being a half of the incoming one, so that:

$$\begin{cases} I_{D_3} = \frac{I}{2} \\ I_{D_2} = \frac{I_{D_3}}{2} = \frac{I}{4} = \frac{I}{2^2} \\ I_{D_1} = \frac{I_{D_2}}{2} = \frac{I}{8} = \frac{I}{2^3} \\ I_{D_0} = \frac{I_{D_1}}{2} = \frac{I}{16} = \frac{I}{2^4} \end{cases} \tag{2.21}$$

The total current entering the feedback resistor on the operational amplifier is:

$$\begin{aligned} I_{R_S} &= \textstyle\sum_{i=0}^{3}(I_{D_i} d_i) \\ &= I \textstyle\sum_{i=0}^{3}(\frac{1}{2^{i+1}} d_i) \\ &= (\tfrac{1}{2}d_3 + \tfrac{1}{2^2}d_2 + \tfrac{1}{2^3}d_1 + \tfrac{1}{2^4}d_0)I \end{aligned} \tag{2.22}$$

with

$$d_i = \begin{cases} 1 & \text{if } D_i \text{ is at logic 1,} \\ \\ 0 & \text{if } D_i \text{ is at logic 0,} \end{cases} \tag{2.23}$$

Since the operational amplifier does not draw current and provides the virtual shortcut, current I_{R_S} entering in R_S results in an output voltage:

$$\begin{aligned} V_{out} = & \quad -R_S I_{R_S} \\ \\ = & \quad -R_S(\tfrac{1}{2}d_3 + \tfrac{1}{2^2}d_2 + \tfrac{1}{2^3}d_1 + \tfrac{1}{2^4}d_0)I \\ \\ = & \quad -V_{ref}\tfrac{R_S}{R}(\tfrac{1}{2}d_3 + \tfrac{1}{2^2}d_2 + \tfrac{1}{2^3}d_1 + \tfrac{1}{2^4}d_0) \end{aligned} \tag{2.24}$$

We obtained an output analog voltage that varies depending on the number and the position of bits at logic 1: when a bit is at logic 1, the DAC outputs a voltage proportional to V_{ref}; if a bit is at logic 0, the portion of output related to that bit is missing. For example, the output referred to the LSB is the one obtainable with $D_0 = 1$ and all other bits at logic 0 (input word: 0001).

It's easy to generalize the result to an N-bit DAC:

$$\begin{cases} I_{R_S} = \sum_{i=0}^{N}(I_{D_i} d_i) \\ \\ V_{out} = -R_S I_{R_S} \end{cases} \tag{2.25}$$

2.4 Printed Circuit Board (PCB)

A *printed circuit board* (PCB) mechanically supports and electrically connects electronic components using conductive tracks etched from copper sheets laminated onto a non-conductive substrate. PCBs can be single sided (one copper layer), double sided (two copper layers) or multi-layer. Conductors on different layers are connected with plated-through holes called vias. On a multi-layer PCB like the one we are going to examine, the components are placed on top and/or bottom layers while power supply and ground are routed with a dedicated layer for each. The ground one is known as *ground plane* and serves as the return path for current from many different components; as we will see, it's a really important component of the PCB. In particular, the front-end board for DarkSide-50 is realized on 4 levels.

Traces impedance

An important consideration is the amount of current carried by the PCB traces. Wider PCB traces are required for higher current densities and for applications where very low series resistance is needed, since the resistance of a conductor is:

$$R = \frac{L}{S}\rho = \frac{L}{W \cdot H}\rho \tag{2.26}$$

where ρ is the resistivity of the material the conductor is made of, L is the lenght of the conductor and $S = W \cdot H$ its section.

When routed over a ground plane, PCB traces form *tranmission lines* and therefore have a defined *characteristic impedance* Z_0. In many design situations characteristic impedance is not utilized, but in the case of high frequency transmission (as in our situation, where rise times are between

1ns and 2ns) or to keep a low noise level, it is necessary to match the load impedance to the line characteristic impedance. In fact, when driving a non-matched load, reflections will occur and this phenomena will distort the signal. Characteristic impedance links current I and voltage V at any point along the line through Ohm's relation:

$$\frac{V}{I} = Z_0 \tag{2.27}$$

so that it is important to know its value. To calculate it, it is useful to remind that a transmission line is associated with a certain amount of series resistance (R) and series inductance (L); plus, each trace exhibits parallel capacitance (C) to the ground plane: the combination oh these elements defines the line's characteristic impedance. The formula with which we calculate this impedance for a lossless line ($R = 0$) is:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.28}$$

Unfortunately, in many cases C and L are unknown values, so we have to follow other steps to calculate the Z_0.

The characteristic impedance is a function of the geometry of the cross section of the line. The formula given in transmission line theory for calculating Z_0 of a PCB trace through its dimensions is:

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \cdot \ln \frac{5.98h}{th + 0.8W} \tag{2.29}$$

where ϵ_r is the relative dielectric constant of the material between the trace and the ground plane, h is the PCB height, W the trace width and th the thickness of the copper.

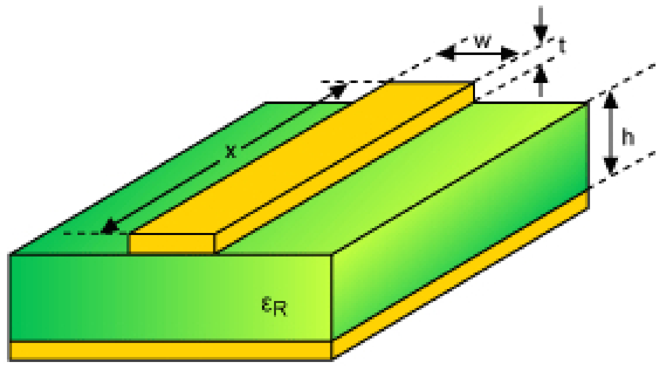


Figure 2.11: PCB trace over the ground plane.

In Fig. 2.11 it's viewable a PCB trace representation with its cross section. Most transmission lines are designed to have 50Ω or 75Ω impedance. The reason is that in many cases the PCB trace has to connect to a cable whose impedance is either 50Ω or 75Ω.

It is useful to notice that often PCB traces have to turn corners. In order to avoid reflection due to the change of the width of the trace, it is important to round corners as much as possible to keep the width constant.

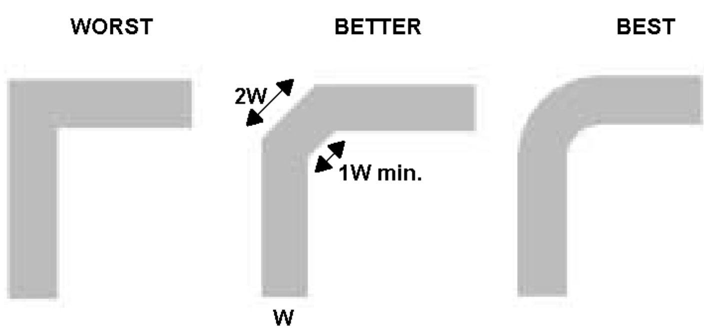


Figure 2.12: Trace corners layouts: rounding has the best effects in avoiding reflection.

Ground planes

The use of ground planes is recommended both for providing a low impedance path to ground and forming effective impedance-controlled transmission lines for the high frequency signal flow on the board.

To conduct the large return currents from many components without significant voltage drops, a plane is used to get a large copper area: as reported in 2.26, its resistance will be very low. By doing so, we ensure that the ground connection of all the components are at the same reference potential, avoiding unwanted noise.

In addition, a ground plane under printed circuit traces can reduce *crosstalk* between adjacent traces. When two traces run parallel, an electrical signal in one can be coupled into the other through electromagnetic induction by magnetic field lines from one linking the other: this is called crosstalk. When a ground plane layer is present underneath, it forms a transmission line with the trace, as already studied in the previous section. The oppositely-directed return currents flow through the ground plane directly beneath the trace. This confines most of the electromagnetic fields to the area near the trace and consequently reduces inductions and therefore crosstalk. Though if it is not our case, when both analog and digital section coexist on the same PCB, ground planes are sometimes split and then connected by a thin trace. This allows the separation of analog and digital sections of the board, in order to avoid noise production in the analog section when a digital component draws its high current from the power supply. The thin trace has low enough impedance to keep the two sides very close to the same potential while keeping the ground currents of one side from coupling into the other side, which

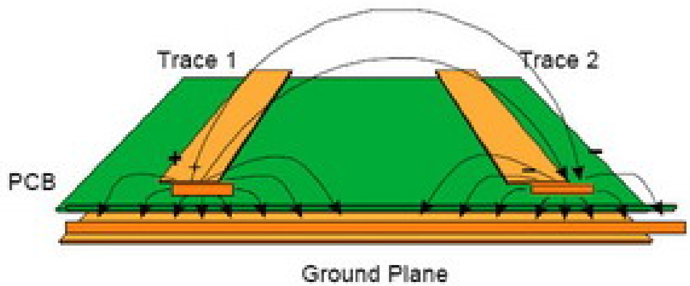


Figure 2.13: Crosstalk between two traces and ground plane effect.

may cause ground loop.

Chapter 3

The Front-End section

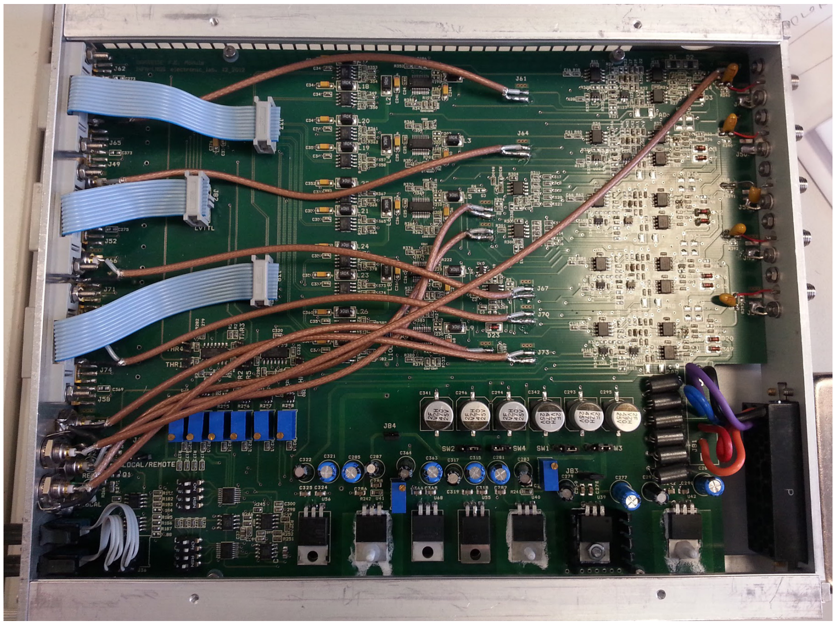
In this chapter will be shown the structure of the front-end section. It is useful to remind that the input signal comes into the front-end from the cold-amp put on the PMT; this is typically a $\simeq -2mV$ signal for a single photoelectron.

3.1 Block Diagram

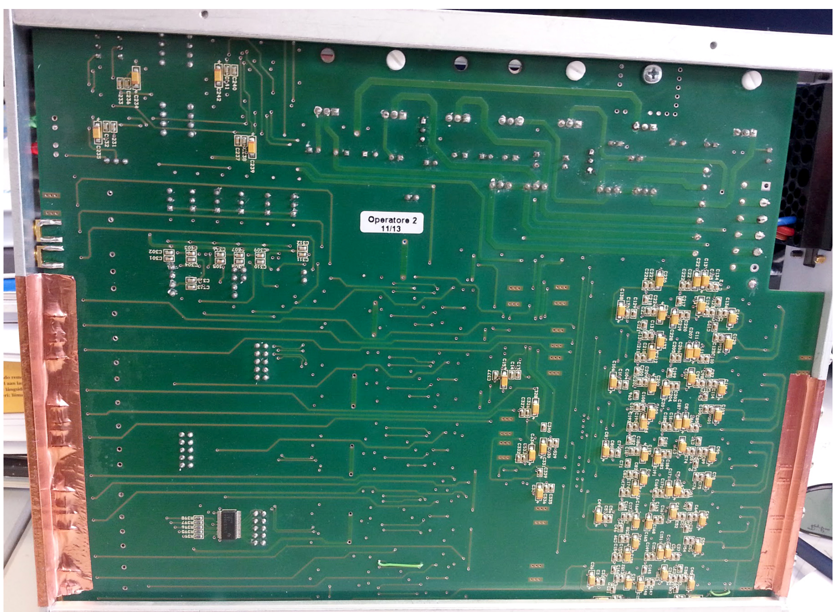
The front-end presents three analog outputs:

- *Fast* - provides a 10x amplification but no filtering;
- *Filtered* - provides a 10x amplification and a low-pass filtering at 100 MHz, making the right conditioning for the 12-bit, 250 MS/s digitizer with 2V dynamic range;
- *Buffered* - provides a buffering and a low-pass filtering at 50 MHz, making the right conditioning for the 14-bit, 100 MS/s digitizer;

A digital LVDS output is provided by using a discriminator with a threshold at about $\frac{1}{4}$ of the single-photoelectron signal. The voltage reference can



(a) Top



(b) Bottom

Figure 3.1: Front-end top and bottom.

be chosen among two possible reference circuits:

- a DAC controlled by an external controller;
- a voltage divider made of trimmer resistors, whose value can be manually framed.

This output goes into a Field Programmable Gate Array (FPGA) which acts as a counter.

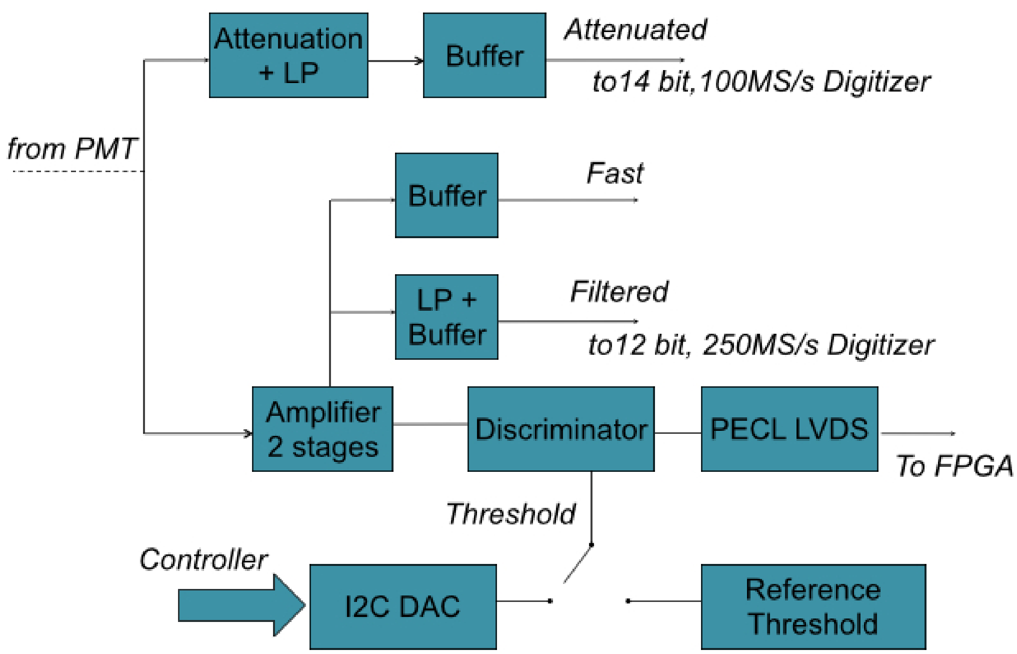
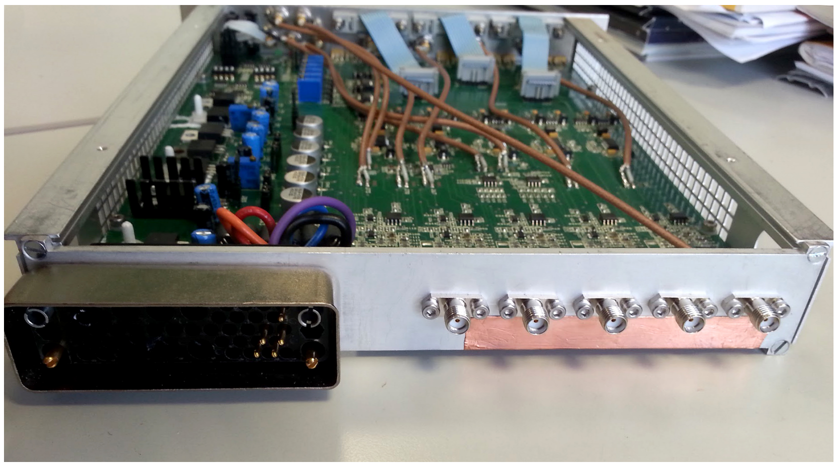
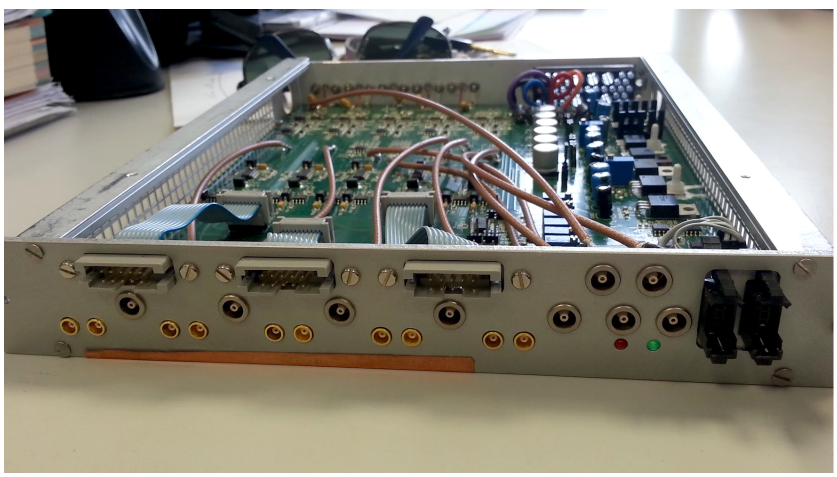


Figure 3.2: Block Diagram of the front-end section.



(a) Inputs



(b) Outputs

Figure 3.3: Front-end inputs and outputs.

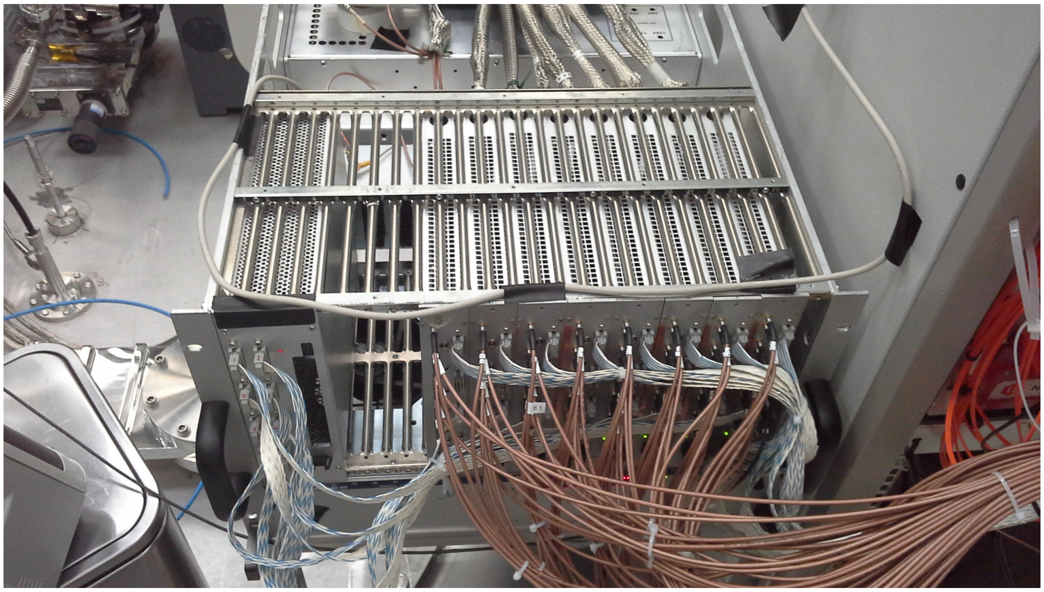


Figure 3.4: The 8 front-end boards in action on the experiment.

3.2 Amplification

1st stage: filtered and fast channels

Both *filtered* and *fast* channels amplifiy the signal of a $\simeq$ 10x factor through a THS3201 operational amplifier in the non-inverting configuration with a $\simeq$ 20x gain, and a termination on a voltage divider made of two 50 Ω resistors, that drops the gain to half the one output by the operational amplifier.

It is important to specify that the THS3201 is a *current* feedback amplifier; in our situation, though, it can be analyzed as if it was a voltage feedback amplifier because of the low feedback impedance.

Looking directly at the circuit in Fig. 3.5, the amplification provided by the operational amplifier can be calculated as follows from 2.9:

$$A_{f1} = 1 + \frac{R_2}{R_1} = 1 + \frac{470\Omega}{22\Omega} \simeq 22 \tag{3.1}$$

For the voltage divider (at the Fig. 4.1 output):

$$V_{filtered} = A_{f1} V_{in} \frac{R_{load}}{R + R_{load}} = V_{in} \frac{A_{f1}}{2} \simeq 11 \tag{3.2}$$

when $R_{load} = R = 50\ \Omega$.

2nd stage: to discriminator

The signal arrives to discriminator amplificated $\simeq$ 40 times: after having passed firstly through the 20x amplification, it goes through another THS3201, in the inverting configuration with a $\simeq$ 4x gain; finally it ends on a voltage divider with the same effect of the one already analyzed.

Using the specified in-circuit values and reported in Fig. 3.5:

$$A_{f2} = -\frac{R_2}{R_1} = -\frac{1000\Omega}{220\Omega} \simeq -4 \tag{3.3}$$

so that the total amplification is

$$A_{TOT} = A_{f1} A_{f2} \simeq 22 \cdot (-4) = -88 \tag{3.4}$$

that after the voltage divider becomes $\frac{A_{TOT}}{2} \simeq -44$.

3.3 Analog outputs: buffering and filtering

Fast output

The *fast* outputs[1] are non-filtered ones. The harmonic content of the input signal is allowed to pass with the sole bandwidth limitation due to the parasitic effects of the electronic components. In effect, on the boards used in DarkSide-50 only one fast output is present: the other was designed because

[1]The upper output in Fig. 4.1 outputs the signal to a sum section not analyzed in this work.

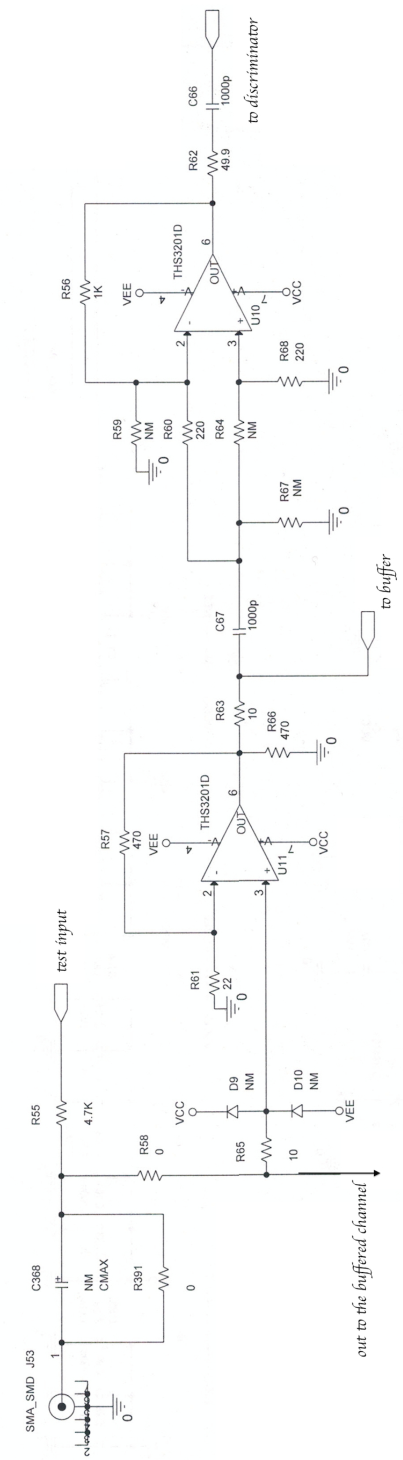


Figure 3.5: The amplification section of the Front-End.

the applied buffer, the LMH6559, can lead multiple loads without efforts; therefore, it is an optional resource designed, but not used on the final board.

As already said, the LMH6559 integrated circuit acts as a buffer: the configuration of the operational amplifier seen in Fig. 2.5 is not directly viewable because the wiring is made inside the chip.

Filtered output

The *filtered* output provides a $\simeq$ 100MHz low-pass filtered output.

The filtering section is made of a RLC low-pass filter with the cut-off frequency given by 2.16:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

that, considering L and C ideal components, gives $f_0 = 98$ MHz. Since the digitizer for the filtered output signal works at 250 MegaSamples/second, the filtering is realized to satisfy the *Nyquist-Shannon sampling theorem*:

> If a function contains no frequencies higher than B Hz, it is completely determined by giving its ordinates at a series of points spaced 1/(2B) seconds apart.

A sufficient sample-rate is therefore 2B samples/second, or anything larger. With a sample-rate lower than 2B, distortion on the reconstruction of the original signal will occur creating what is called *aliasing*: unwanted frequencies will show up in the reconstructed signal spectrum. With a maximum frequency of 100 MHz, sample-rate should be at minimum 200 MegaSamples/second (MSps): 250 is larger, so that the filtered output can be converted without problems.

The buffering circuit is realized with the LMH6559 as explained in the previous lines. As viewable in Fig. 4.1, feedback resistors for it are designed but not mounted on the board: the LMH6559 can be used also as an operational amplifier, if desired. This versatile configuration is called *footprint mixed*.

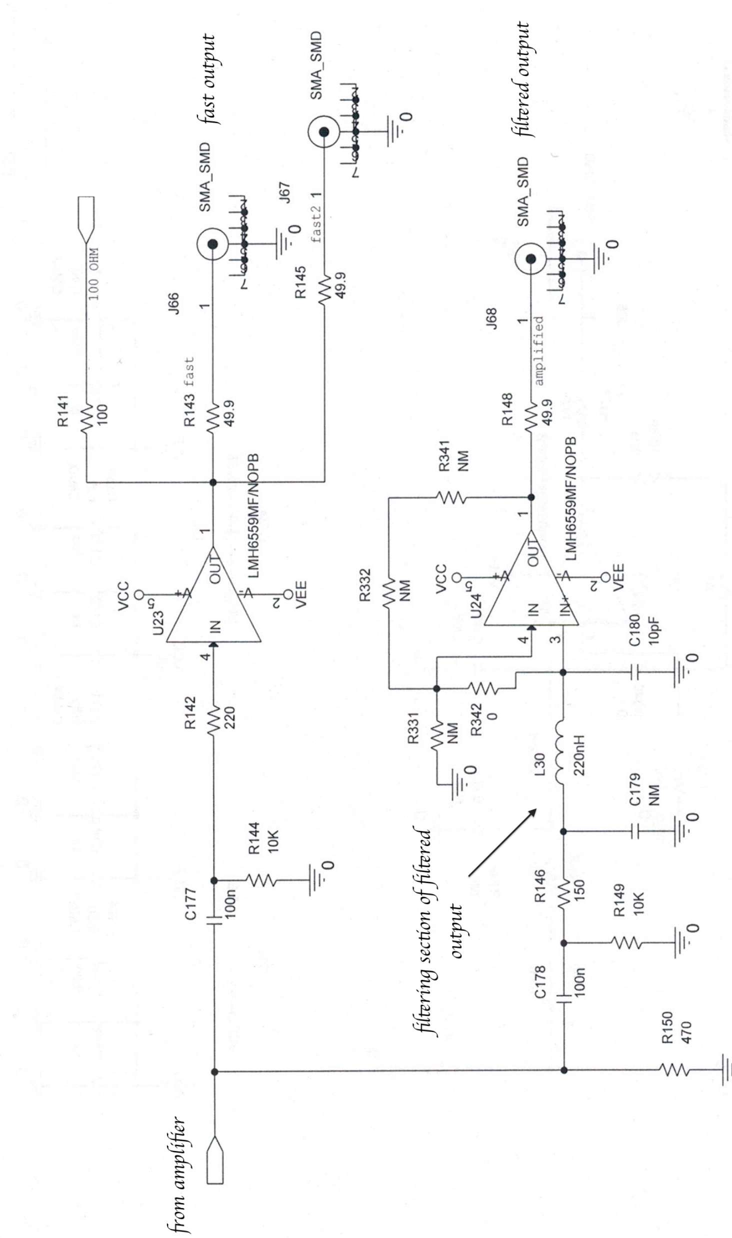


Figure 3.6: The buffering and filtering section of the Front-End for amplified outputs.

Buffered output

The buffered output provides a 50MHz low-pass filtered output. The buffer is realized through a non-inverting operational amplifier, the THS3061 with $R_1 = R_2$. It was not used a normal buffer because the operational amplifier has a smaller bandwidth, and therefore reduces the noise (see Appendix A). For the 2.9 its gain is

$$A_f = 1 + \frac{R_2}{R_1} = 2$$

that with the voltage divider becomes a unity gain.

The filtering is due to the THS3061 itself. In fact, configured with a 2x gain it acts as a low-pass filter. The cut-off frequency results to be variable with the feedback resistor value R_f: in Fig. 3.7 there are transfer functions for three different values of R_f. The 82Ω and the 820Ω resistors are there because a filter could have been realized with those; in effect, when the measurements were done, it turned out to be sufficient the sole THS3061. As we will see later, the two resistors will contribute for a fraction of the total noise level of the buffered output.

The value of 50MHz allows the digitizer of the buffered output to work without generating aliasing, since its sample-rate is of 100 MS/sec.

The choice of the THS3061 is not casual. First, it is important to specify that the buffered section is on the board to allow the detection of large signals: in fact, as said in Chapter 4, the filtered and fast channels start to saturate with a $\simeq$ 200mV input signal because of the power supply[2]. Big signals need therefore to be detected through the buffered channel: the THS3061 has a

[2]When amplified, a 200mV signal becomes a 2V signal: since the dynamic range of the digitizer is 2V, this is perfectly performing.

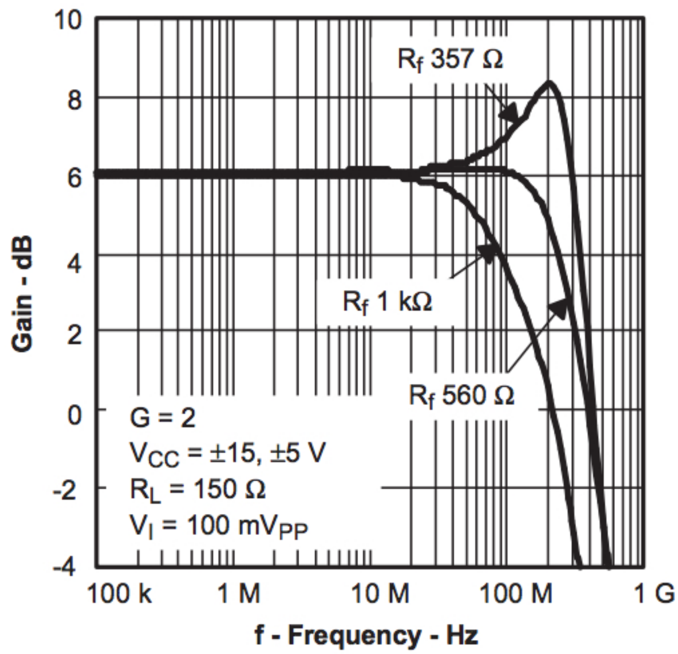


Figure 3.7: THS3061 transfer functions for $R_f = 357\ \Omega$, $560\ \Omega$ and $1000\ \Omega$.

wide dynamic range, making it the ideal choice for this purpose. Then, it is stable with a 2x gain, while the THS3201, in example, is not. A problem of this chip is the small amount of output current that forces to have a not so small R_1 resistor of 750Ω, producing unvoidable noise[3].

3.4 Digital output: threshold and discriminator

3.4.1 Threshold

Voltage reference

Since the discriminator's threshold is the basis of the analog to digital convertion, it is very important to provide a really *precise* and *stable* voltage reference.

To reach a high precision we need a really low noise level on the voltage reference; having a good stability refers mostly to have a really low variation of the reference with the temperature. The LM4140 has these characteristics, with:

- ultra low noise, with $V_{Noise} \simeq 2.2\mu V$ peak to peak;
- ultra low temperature-related variation, with 3 ppm per Celsius grade.

As we have seen before, there are two ways among which can be choosed the threshold-generation for the discriminator. Both of them uses a voltage reference made with the LM4140 as in Fig. 3.9.

[3] The LNGS electronic division is currently working on techniques to improve the noise rejection for this issue.

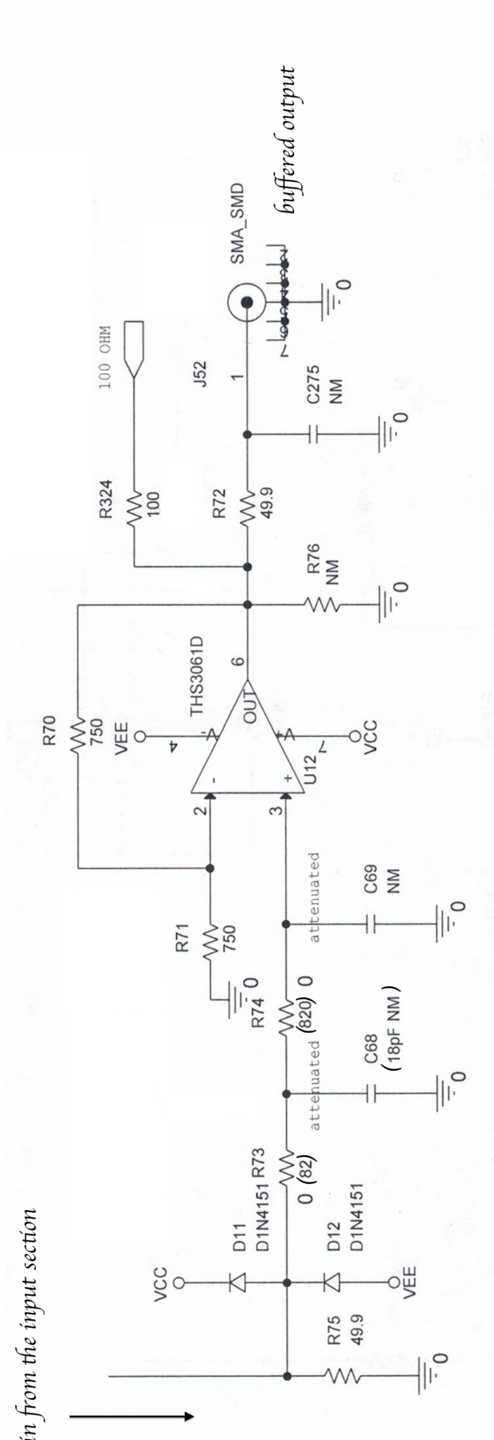


Figure 3.8: The buffering and filtering section of the Front-End for the buffered output.

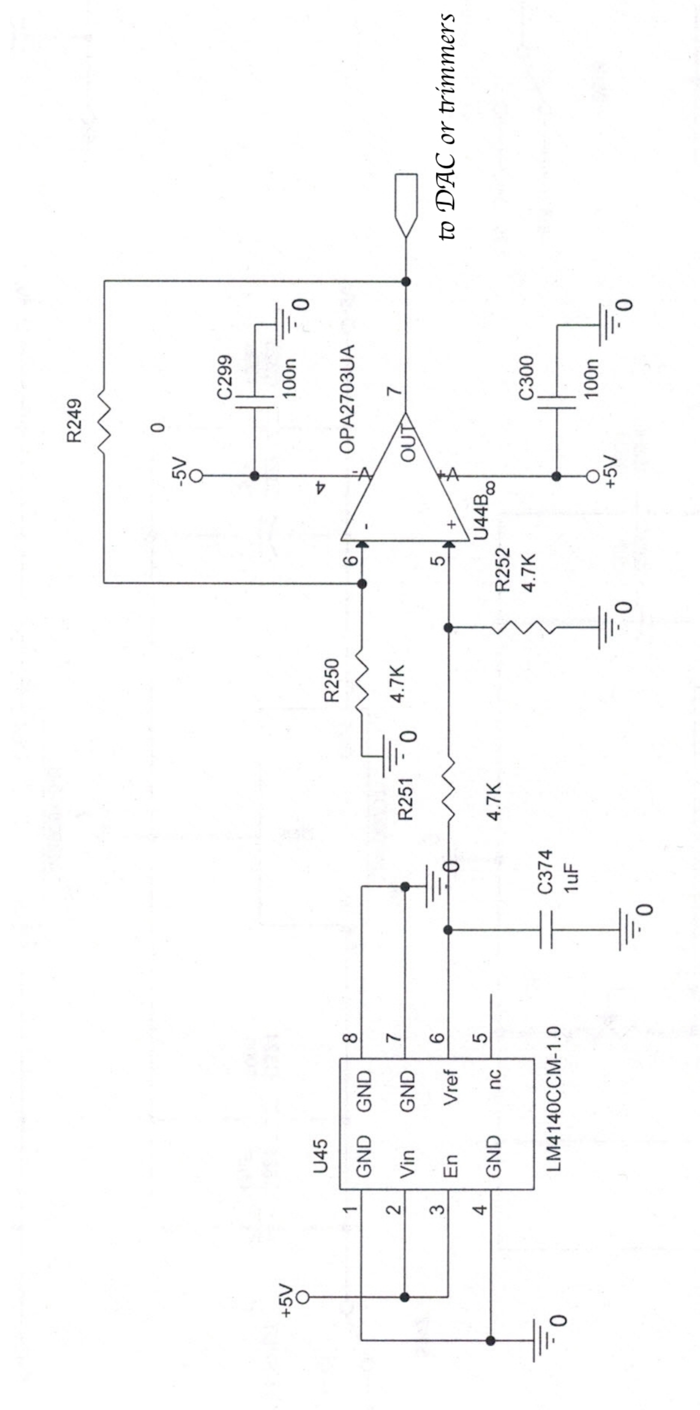


Figure 3.9: The voltage reference generation: the LM4140 and its buffering stage.

Threshold: DAC

The first way we will cover is the one with DACs. We already covered the working principles of a DAC in 2.3 (page 33): the ones used in the front-end are MAX5116, 8-bit DACs with 4 outputs. The voltage reference is made with the circuit seen in the previous section.

A remote controller sets the bits of the word to convert through an I2C bus, that works with two serial lines:

- SDA: is the line through which sending the input data (in our case, the 8-bit word to convert);
- SCL: is the line for the controller's clock, through which controlling the actions.

In order to communicate with the controller, the DAC has a precise 8-bit address, of which 4 bits are factory-stored and the other are manually set with the SW DIP-4, viewable in Fig. 3.10. It is a collection of 4 switches manually controlled that let the user put 4 respective nodes to a voltage or another. In this case it is used to fix 4 of the 8 bits of the DAC index manually, by putting them at logic 1 (obtained with the showed voltage supply at 5V and a resistor) or logic 0 (connecting the node to ground).

Threshold: trimmers

The second way to make the threshold is to use on-board variable resistors, commonly known as *trimmers*.

Trimmers have 3 pins: 2 fixed ones used to connect the entire resistor among two voltages and 1 mobile one to capture the tension from a certain

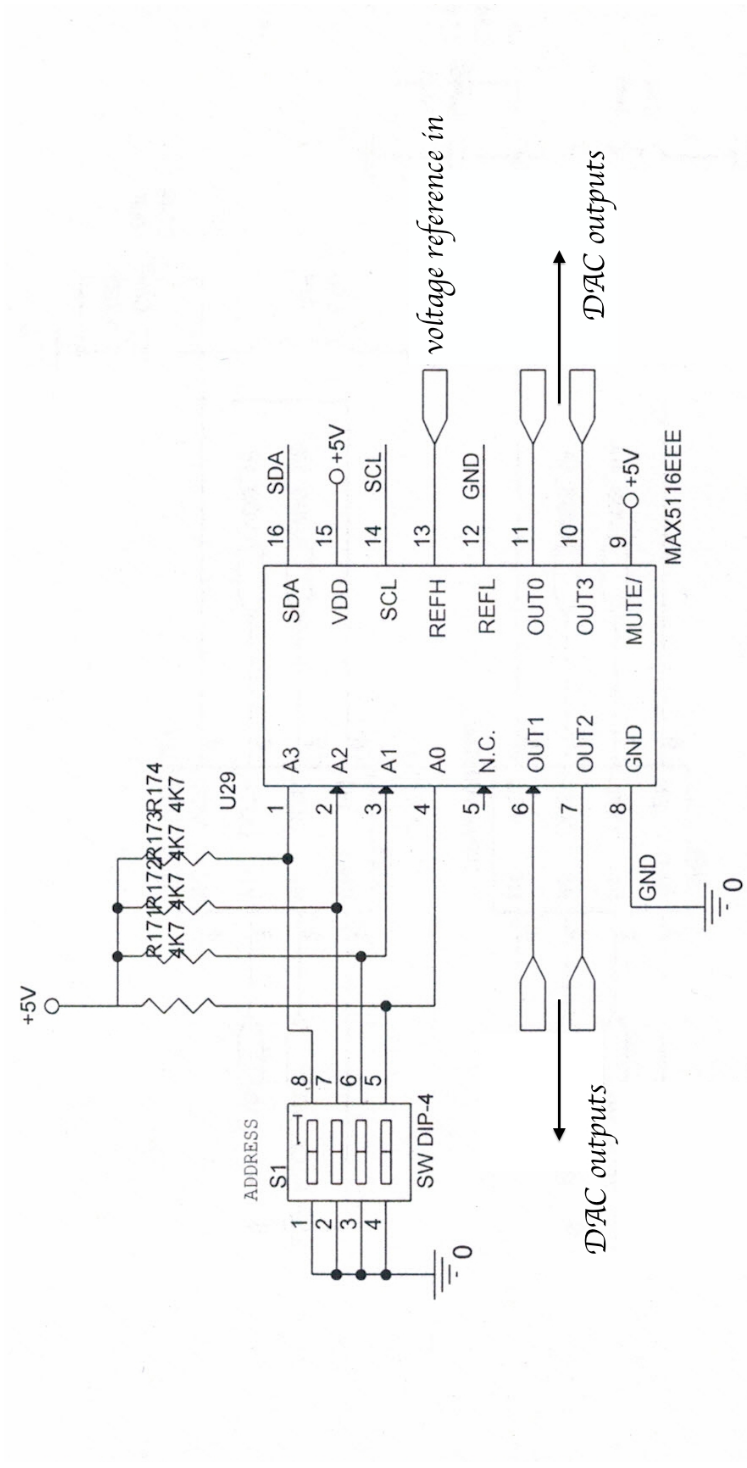


Figure 3.10: The MAX5116 DAC with DIP switch, for the automated control of threshold.

point in the length the resistor. Since its resistance value is given by the 2.26, changing the capturing point is like using a variable resistor with the important result of a constant current in the resistor itself. In Fig. trimmers is shown the circuit for the trimmers used in the front-end[4].

Trimmers are manually controlled by the user, therefore the main purpose of this section is to use them locally, for specific situations in which a direct control is needed.

[4]Though each board has 5 channels on it, there is also a sum channel with a discriminator which we will not talk about: this is the reason for the 6th trimmer.

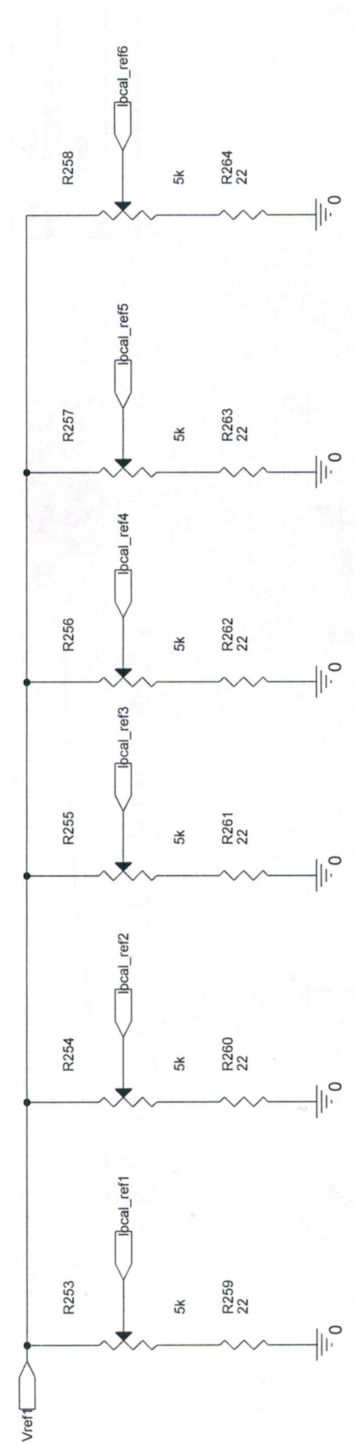


Figure 3.11: The trimmers for the manual control of threshold.

Selection of the threshold

Having explained the two ways of making the threshold, we will now study how to select one of them with a *multiplexer*. The concept is simple: a switch can output both the remote or the local threshold under control of a logic input - a bit. Depending on the state of the bit (logic 1 or 0), one or the other input signal will pass. Such device is called multiplexer, and in our case it has got two inputs and one control bit, acting as a simple switch. But more in general, a multiplexer can work with 2^N signals controlled by N bits.

In the front-end TS5A3160 multiplexers are used. Calling the signals to be selected I_{NO} and I_{NC} (in relation to Fig. 3.12), and IN the control bit, the TS5A3160 output (called COM) acts as follows:

$$COM = \begin{cases} I_{NO} & \text{if IN is at logic 1,} \\ \\ I_{NC} & \text{if IN is at logic 0} \end{cases} \tag{3.5}$$

In our case, we are going to see that logic 1 equals to a 5V voltage, and logic 0 to 0V. In fact, the control bit is generated through a BJT (Q_1 in Fig. 3.12), NPN transistor whose gate voltage is controlled by a jumper. The jumper is a "mobile shortcut": it is simply a piece of conductor manually placeable on two pins to shortcut them. The jumper can connect the gate to a 5V voltage supply or to 0V (ground). When the 5V voltage is on, the gate-emitter junction of Q_1 gets directly polarized so that Q_1 acts as a current amplifier: the maximum current is drawn from collector to emitter and the Q_1 collector is at 0V. Otherwise, when 0V are on the gate, Q_1 collector is at $V_{CC} = 5$V because no current is drawn between collector and emitter since the gate-emitter junction is inversely polarized. It is clear now that the collector is our control bit. The BJT acts as a switch:

$$IN = \begin{cases} 0 & \text{if } Q_1 \text{ is ON,} \\ \\ 1 & \text{if } Q_1 \text{ is OFF} \end{cases} \tag{3.6}$$

Finally, two LEDs (D_{21} and D_{22} in Fig. 3.12) let the user know which threshold is being used.

The BJT Q_2 has its gate at Q_1 collector's voltage, so that if Q_1 is ON the jumper is connecting its gate to 5V and will make D_{21} emit light, while Q_2 is off avoiding D_{22} to emit light. Otherwise, if Q_1 is OFF, D_{22} will emit light and D_{21} will not. Summarizing:

Q_1	Q_2	**Threshold**
ON	OFF	Local
OFF	ON	Remote

Threshold buffering

A buffer section follows each multiplexer. The buffering is realized through non-inverting operational amplifiers with $R_1 = R_2$.

3.4.2 Discriminator

Finally, the discriminator comes into play. We have already seen how the signal to be discriminated is conditioned in Par. 3.2; in the discriminator it is comparated to the threshold, with an output similar to the one shown in Fig. 2.6. The device used is a ADCMP552: it features a 500ps propagation

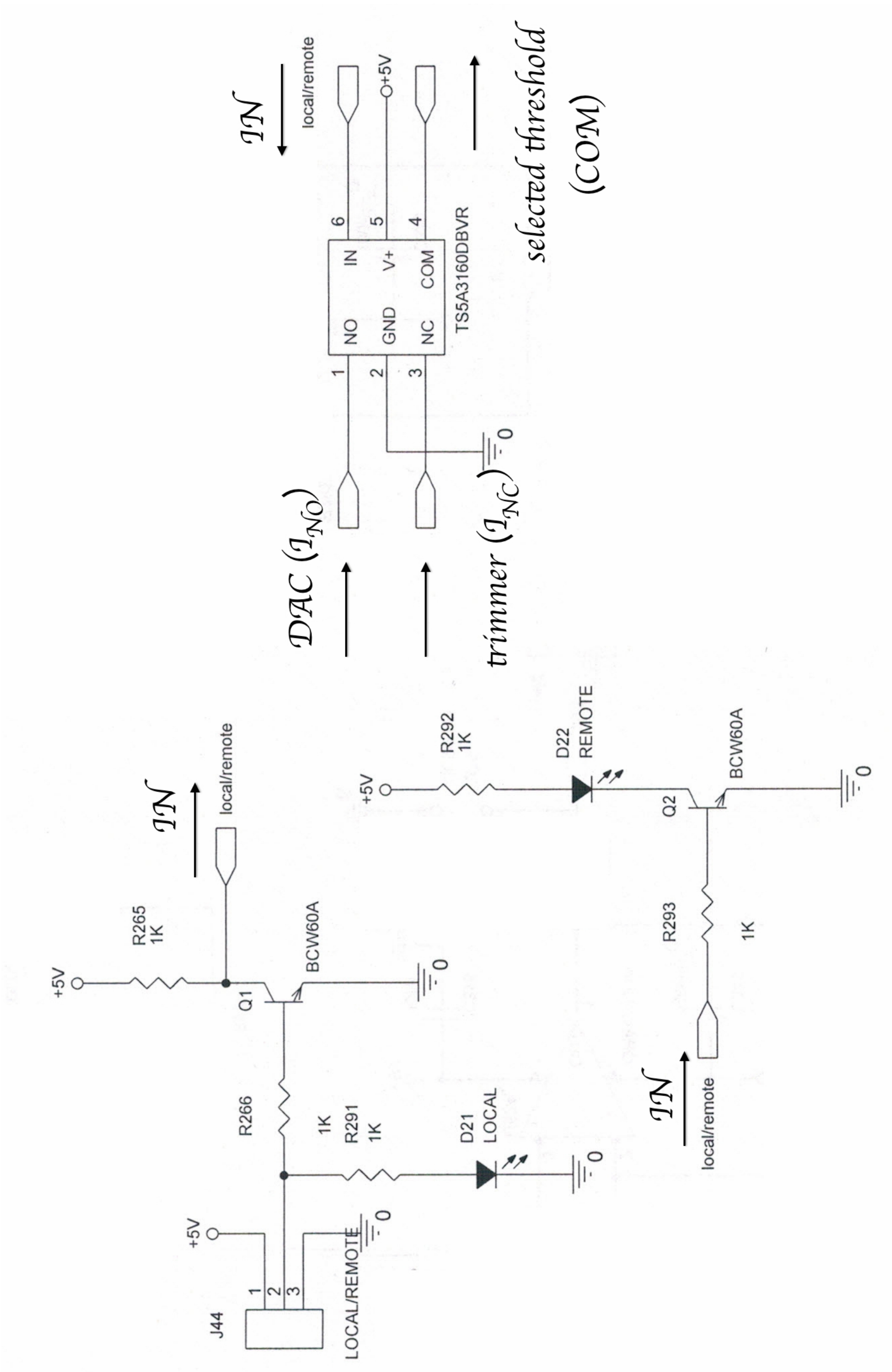


Figure 3.12: Threshold selection: the TS5A3160 switch and its control bit's generation.

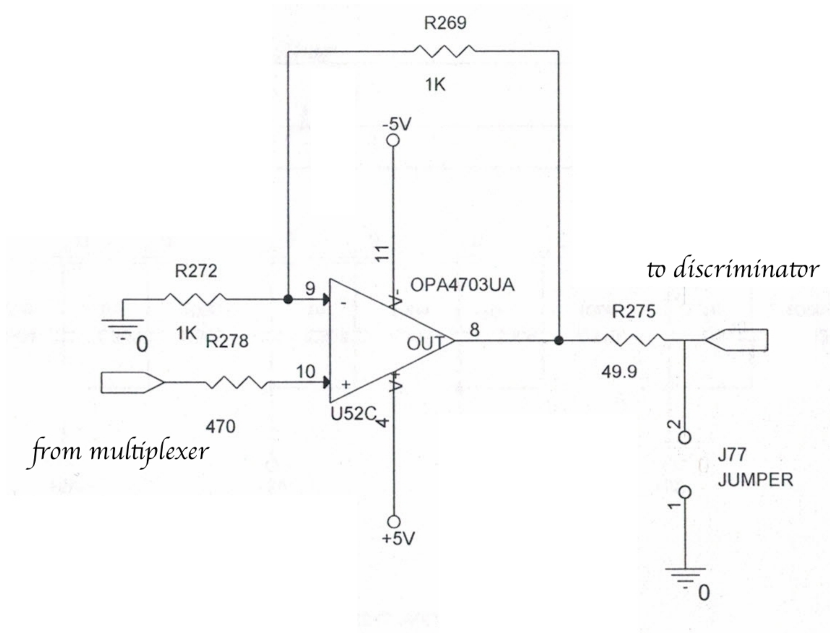


Figure 3.13: Threshold buffering with a non-inverting operational amplifier.

delay with less than 125ps overdrive dispersion[5], being a very high speed comparator. The most critical aspect about working with high speed devices is the use of a low impedance ground plane: as seen in Par. 2.4, it provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused by ground bounce. A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

Then, minimizing resistance from the signal source to the comparator input is necessary in order to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the

[5]Overdrive dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed.

amplitude of high-frequency signals.

The addition of *hysteresis* to a comparator is often useful in a noisy environment or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Fig. 3.14. If the input voltage approaches the threshold from the negative direction, the comparator switches from a 0 to a 1 when the input crosses V_{ref_+}. The new switching threshold becomes V_{ref_-}. The comparator remains in a 1 state until the V_{ref_-} threshold is crossed coming from the positive direction. In this manner, noise centered on 0 V input does not cause the comparator to switch states unless it exceeds the region bounded by V_{ref_+} and V_{ref_-}. Positive feedback from the output to the input is often used to produce hysteresis in a comparator: in the ADCMP552, hysteresis is generated through the programmable hysteresis pin. A resistor from the it pin to voltage supply creates a current into the part that is used to generate hysteresis. Both the direct and the inverted output are used to have a LVDS signal.

3.5 Noise-reduction techniques

We already mentioned that it is very important for the DarkSide-50 experiment to have low-noise electronic signals. A variety of techniques are adopted in the front-end design to satisfy this requirement: we have already said something about particular chips before, but in this section we will spend some more words on the general principles of noise reduction.

First of all, low-noise active components were used. Secondly, keeping low trace impedance helps to keep a low noise. Then, where possible the

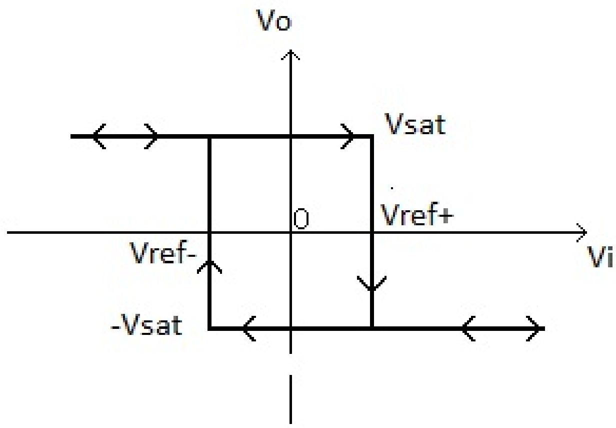


Figure 3.14: Transfer function for a comparator with hysteresis.

bandwidth of the circuits is reduced: as specified in A.5, the smaller the noise bandwidth, the lower its power. This is accomplished mainly using filters.

We will now give some examples of these practices. In the THS3201 used for the 20x gain, a small resistor of 22Ω is placed on the non-inverting input: it generates a low thermal noise (see A.7). A similar treatment is not possible on the buffered channel where the THS3061 was needed, because it has a low output current not able to sustain small resistors. Though, THS3061 naturally has a small bandwidth, making the noise reduced.

A clever example of filtering in order to reduce noise is in the buffers for the fast channels. On the LMH6559 input is viewable an apparently useless resistor: actually, it is used with the parasitic capacitance ($\simeq$ 2pF) of the chip to realize a low-pass filter. A brilliant idea to take advantage of a flaw!

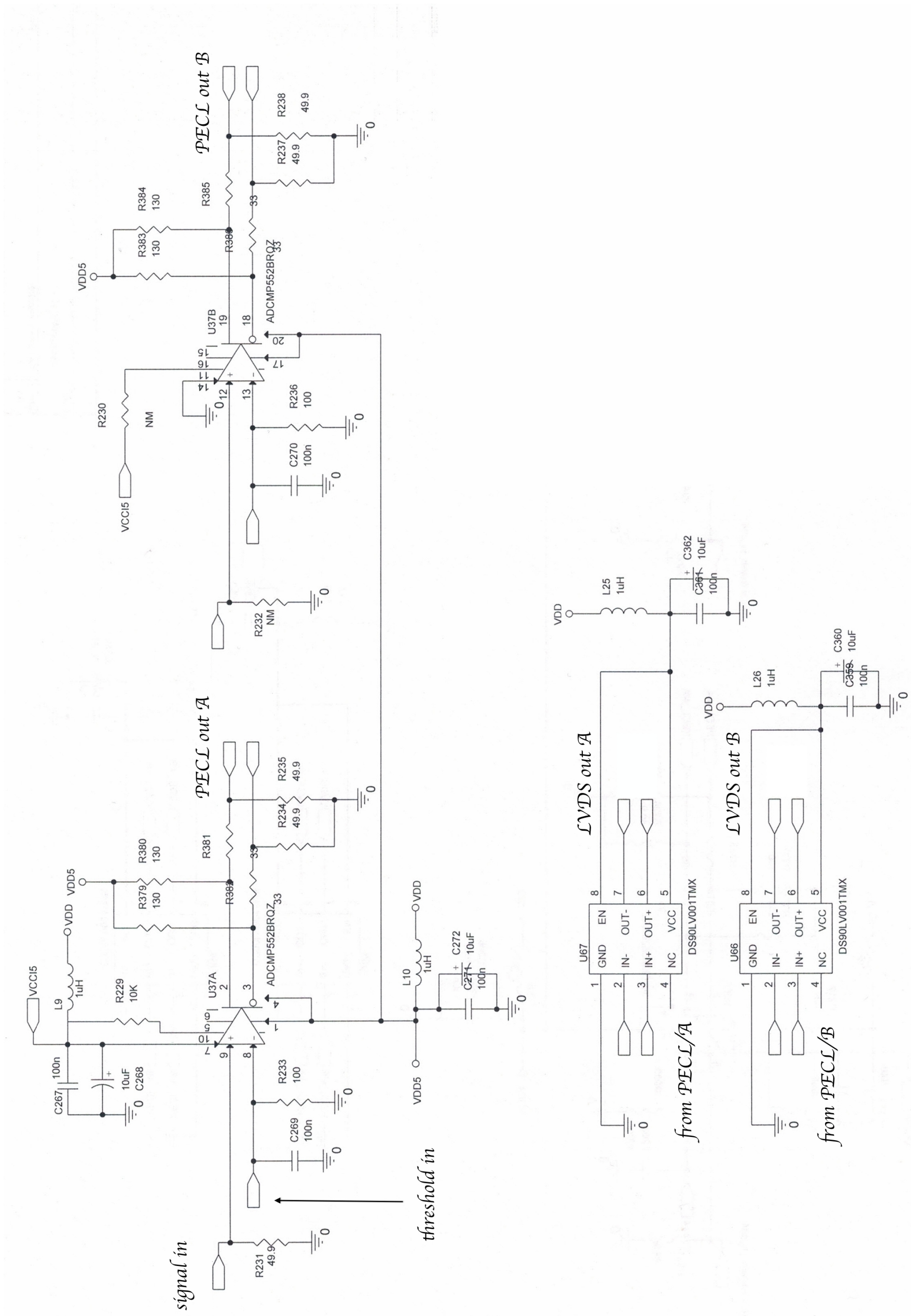


Figure 3.15: The ADCMP552 discriminator and PECL to LVDS conversion.

Chapter 4

Measures

4.1 Amplification and fall time

To measure amplification and fall time[1] of the output was used a pulse as input, with a transition time of 1ns.

The instruments involved in the measure were:

- Philips PM 5785B *pulse generator*
- Rohde & Schwarz RTO 1024, 2Ghz, 10GS/s, *digital oscilloscope*
- NIM crate for the front-end placement

A PSC-2R-42 power divider was also used to split the input signal to allow the view of the input, in addition to the output, on the oscilloscope.

Figures from 4.2 to 4.11 show amplification of the three channels through screenshots from the oscilloscope with a variety of input levels. The blue signal is the input, the pink one is the output. On the high-left corner there are the windows with input and output values. The maximum output level

[1]Fall time is the time taken by a signal to go from 10% to 90% of its stable value.

Figure 4.1: The NIM crate for the front-end placement.

reachable is $\simeq$ 2V because of the power supply. In that region, in fact, the amplifier starts to saturate, as Fig. 4.5 demonstrates.

Figures from 4.12 to 4.14 show fall time measurements for each channel. It is interesting to notice that we can approximately forecast the result of the bandwidth measure using fall time. In fact, there is a relation (that won't be demonstrated in this work) between fall time and the maximum frequency allowed to pass (in other words, the bandwidth) in a system:

$$BW \simeq \frac{0.35}{\text{Fall Time}} \tag{4.1}$$

In the following sections will be shown the measurements results, and calculated the expected bandwidth for each channel: we will later compare these results with realized measures.

Fast output

Input (mV)	**Output (mV)**	**Fall Time (ns)**
20	197	
51	489	1.61
126	1220	
190	1840 (saturation)	

$$BW \simeq \frac{0.35}{1.6 \cdot 10^{-9}s} \simeq 218\text{MHz} \tag{4.2}$$

Filtered output

Input (mV)	Output (mV)	Fall Time (ns)
30	308	
76	766	3.37
187	1840 (practically in saturation)	

$$BW \simeq \frac{0.35}{3.4 \cdot 10^{-9} s} \simeq 103\text{MHz} \tag{4.3}$$

Buffered output

Input (mV)	Output (mV)	Fall Time (ns)
77	73	
188	177	7.29
487	453	

$$BW \simeq \frac{0.35}{3.9 \cdot 10^{-9} s} \simeq 48\text{MHz} \tag{4.4}$$

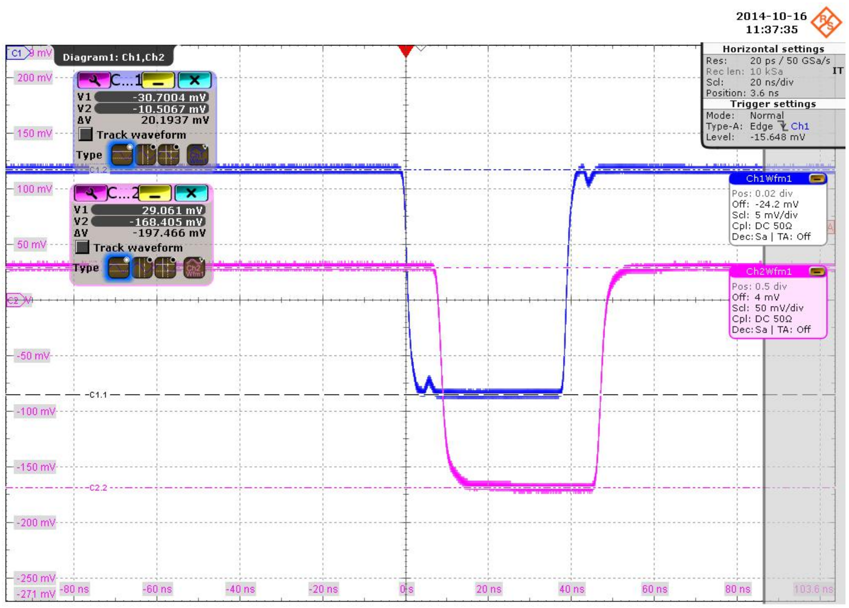


Figure 4.2: Fast output with 20 mV in input.

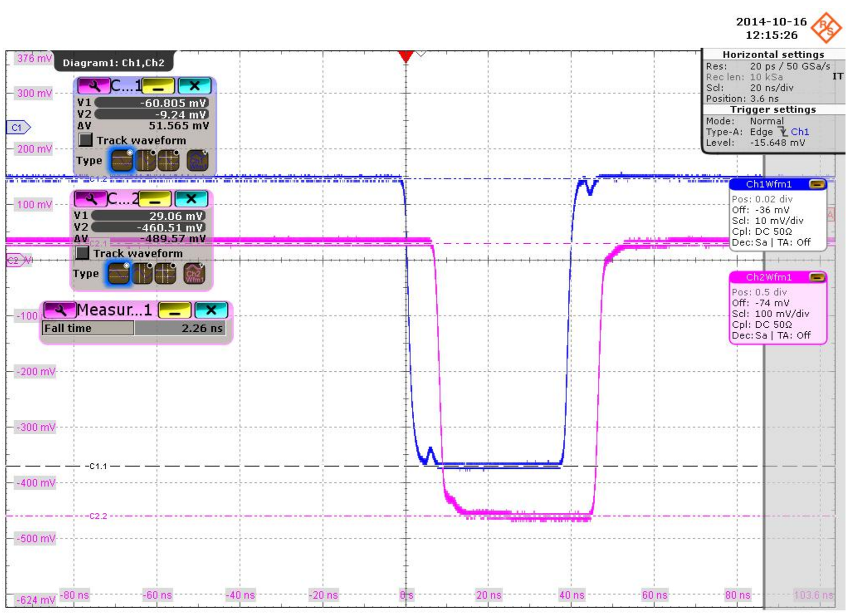


Figure 4.3: Fast output with 51 mV in input.

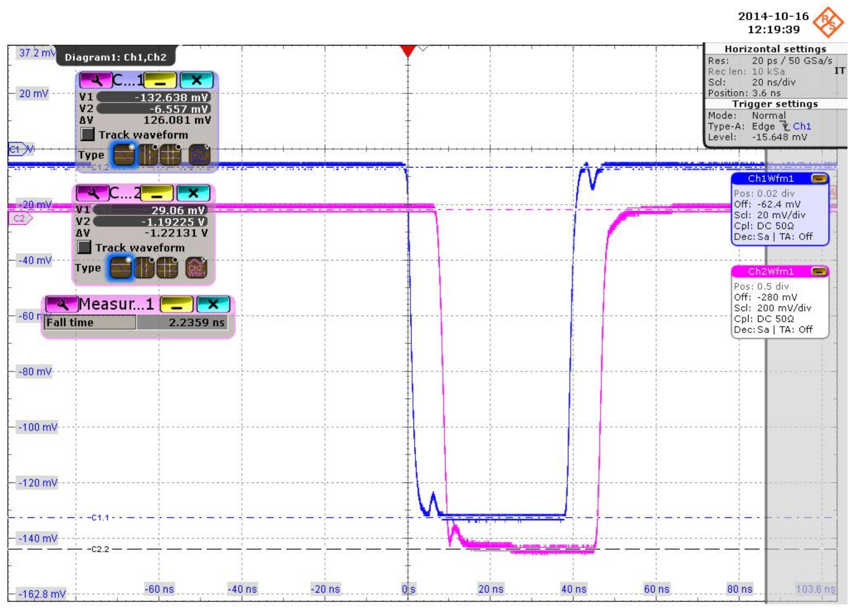


Figure 4.4: Fast output with 126 mV in input.

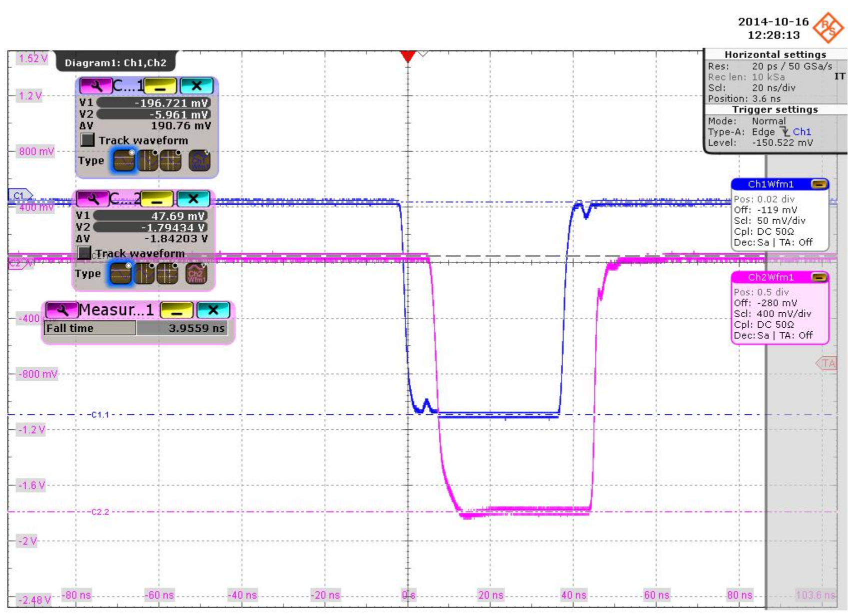


Figure 4.5: Fast output with 190mV: beginning of saturation.

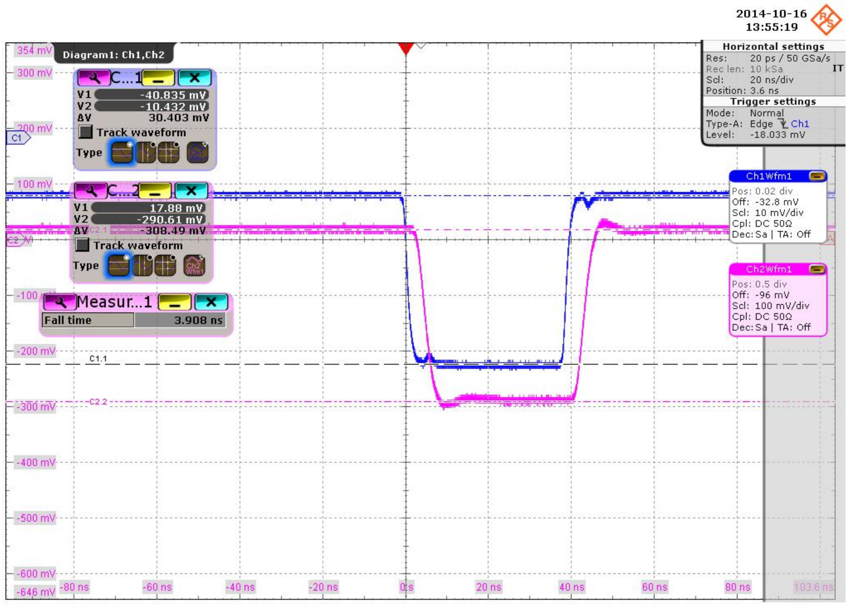


Figure 4.6: Filtered output with 30 mV in input.

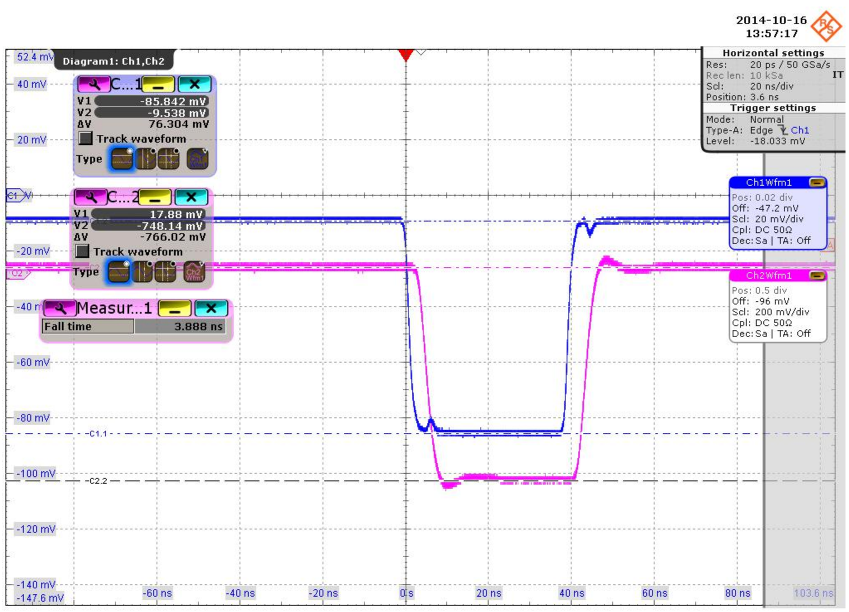


Figure 4.7: Filtered output with 76 mV in input.

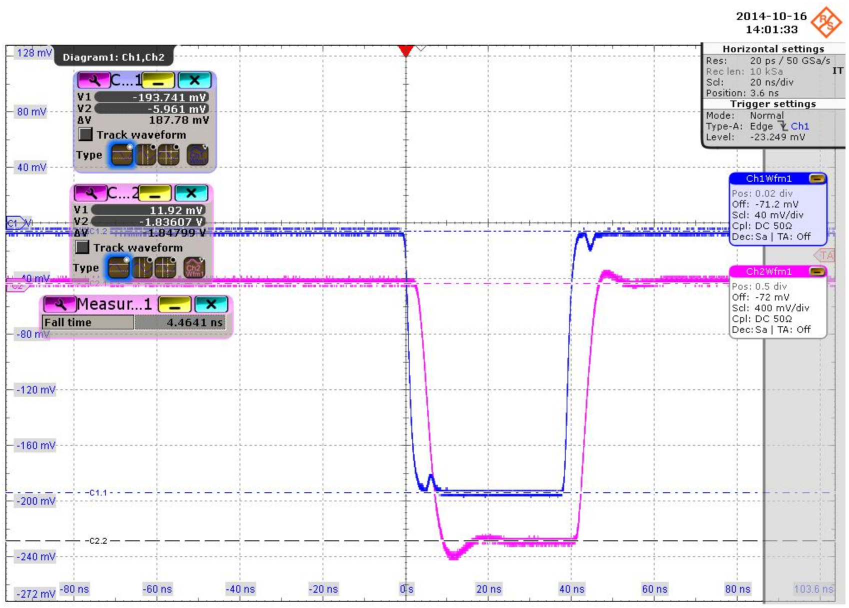


Figure 4.8: Filtered output with 187 mV in input.

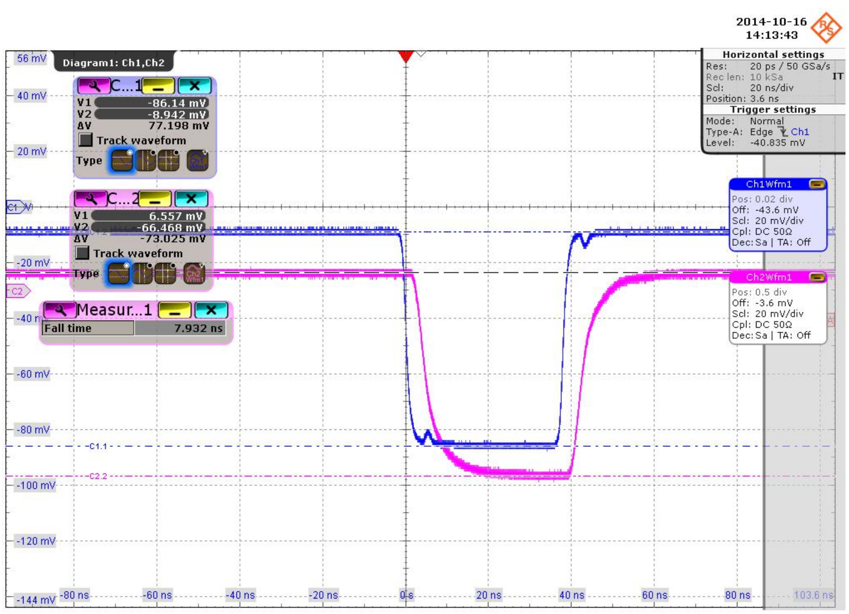


Figure 4.9: Buffered output with 77 mV in input.

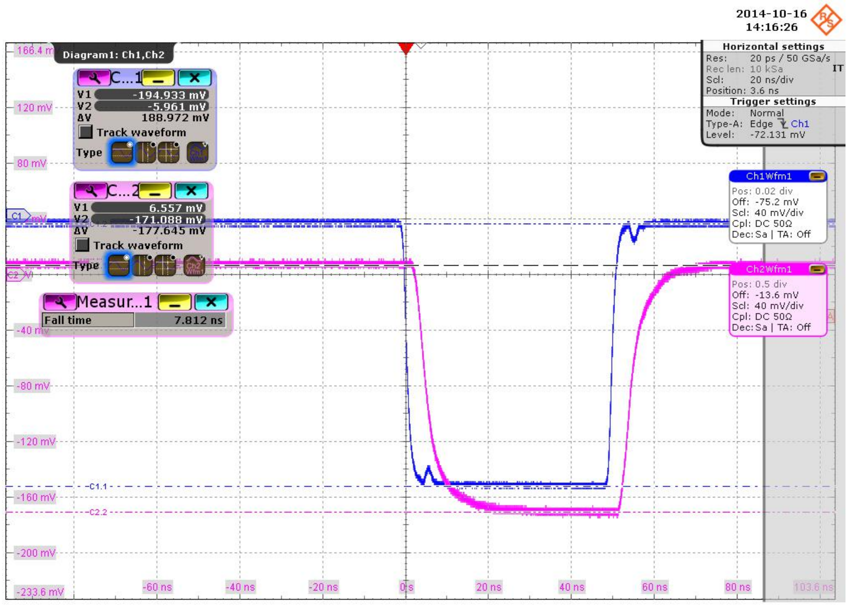


Figure 4.10: Buffered output with 188 mV in input.

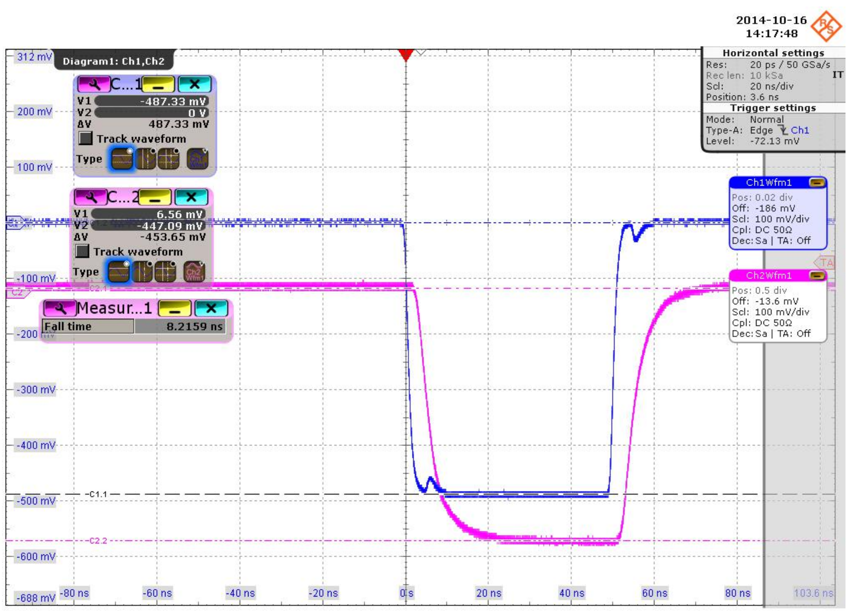


Figure 4.11: Buffered output with 487 mV in input.

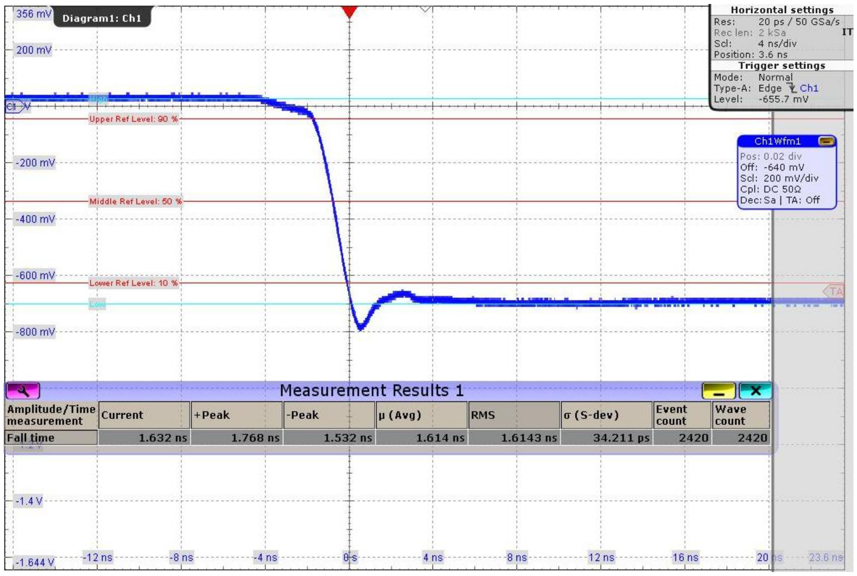


Figure 4.12: Fall time of the fast output.

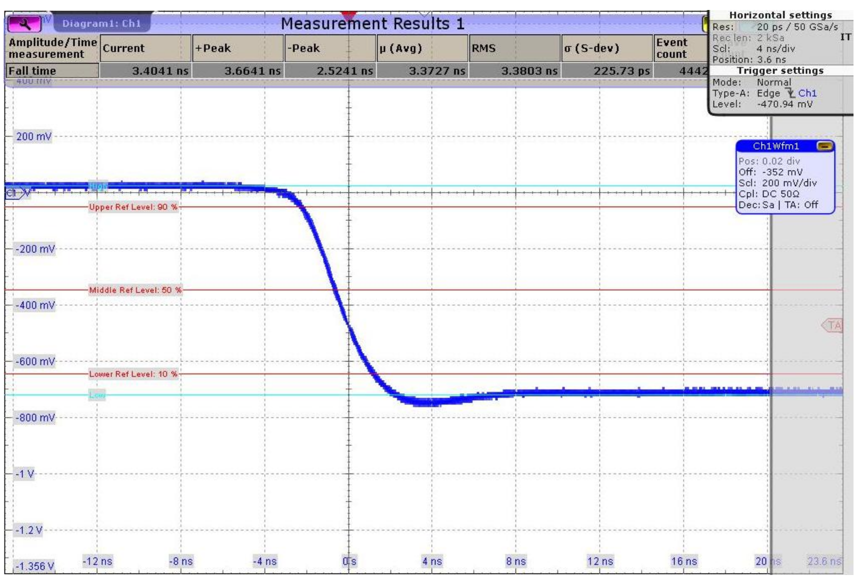


Figure 4.13: Fall time of the filtered output.

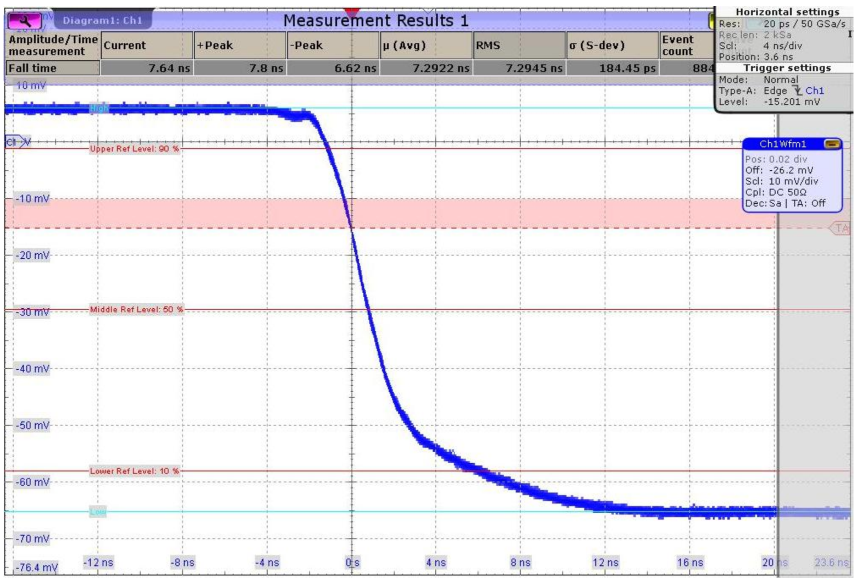


Figure 4.14: Fall time of the buffered output.

4.2 Bandwidth

To measure the bandwidth was used a Keysight ENA 5071c, 9kHz-8.5GHz, vector *network analyzer*: practically, it shows the transfer function of the channels.

On the acquired screenshots is viewable the transfer function and, on their high-left angle, the value of the frequency in correspondence to the marker position (directly shown on the transfer function and placed on -3dB to measure the cut-off frequency). To make it easier to compare the different outputs, in the filtered and in the buffered screenshots is viewable the fast output transfer function left on the background.

We can see that each channel works very well:

- Fast output
  - Amplification: 20 dB
  - Bandwidth: 282 MHz
- Filtered output
  - Amplification: 20 dB
  - Bandwidth: 97 MHz
- Buffered output
  - Amplification: 0 dB
  - Bandwidth: 50 MHz

The amplification values are as expected, since a 10x amplification equals to a difference of 20dB between output and input.

The bandwidth measurements reveal values slightly different than approximately calculated in 4.2, 4.3 and 4.4, which remain anyway good instruments to have an idea of what is going on in the system.

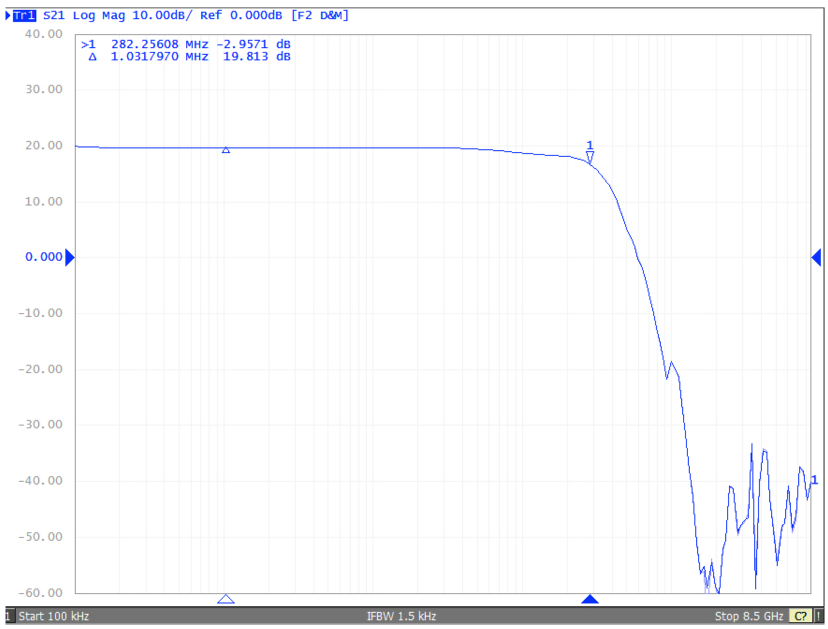


Figure 4.15: Transfer funcion of the fast output.

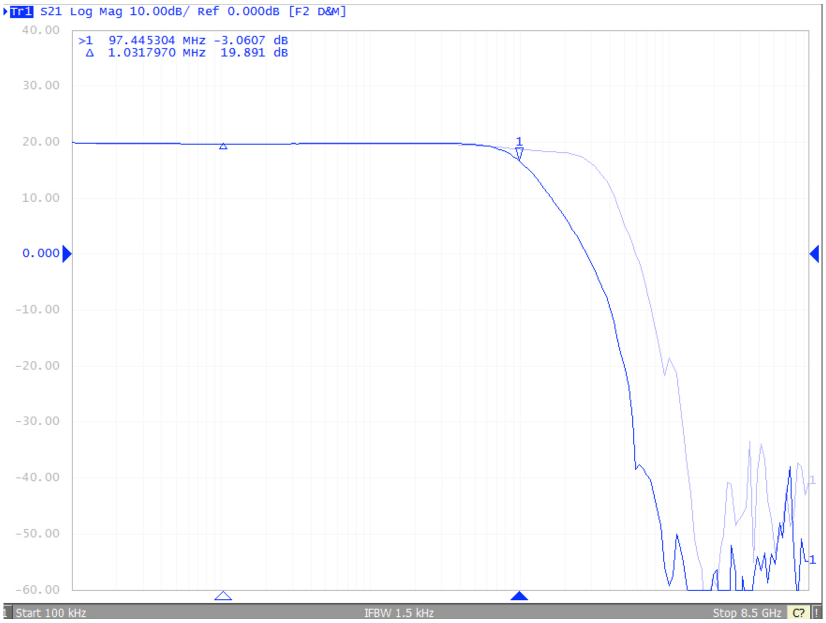


Figure 4.16: Transfer funcion of the filtered output.

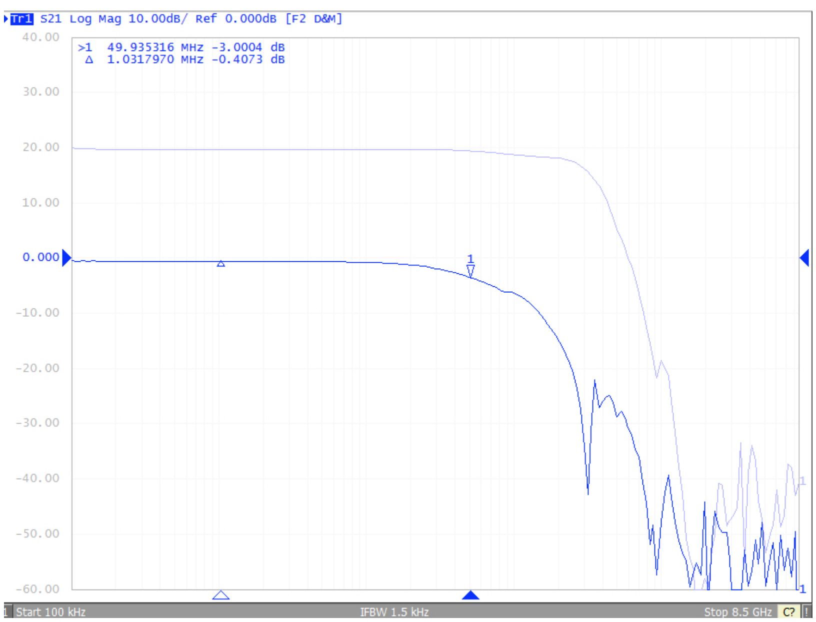


Figure 4.17: Transfer funcion of the buffered output.

4.3 Noise

To measure the noise level were used two instruments:

- Rohde & Schwarz RTO 1024, 2Ghz, 10GS/s, *digital oscilloscope*
- Rohde & Schwarz FSV, 7GHz, signal and *spectrum analyzer*

The outputs of the front-end were directly connected to the instruments. The results are stunning:

- Fast output: 247 μV
- Filtered output: 196 μV
- Buffered output: 164 μV

So the noise level is extremely low on each channel.

To give an example on how to evaluate noise for an operational amplifier considering both Johnson noise and the one caused by the amplifier's input noise current, we will now analyze the buffered output. First, calculate the Johnson noise for each input of the amplifier. Since $v_{J_{R_1}} = v_{J_{R_2}}$, for the inverting input we have:

$$v_{J_-} = 2\sqrt{4K_BTR\Delta f} = 2\sqrt{4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 750 \cdot 50 \cdot 10^6} = 2{\cdot}25\mu V = 50\mu V$$

For the non-inverting one:

$$v_{J_+} = \sqrt{4K_BTR\Delta f} = \sqrt{4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 900 \cdot 50 \cdot 10^6} = 27\mu V$$

Then we have to consider the noise caused by the input noise current of the amplifier, specified in the datasheet to be 36pA for the inverting input and 20pA for the non-inverting one. Considering a dynamical analysis, the equivalent resistance is 325Ω from the inverting input and 900Ω from the non-inverting one. Therefore, these noise contributes are:

$$v_{IN_-} = 36 \cdot 10^{-12} pA \cdot 325\Omega = 11nV$$

$$v_{IN_+} = 20 \cdot 10^{-12} pA \cdot 900\Omega = 18nV$$

Calculating the RMS value:

$$v_{noise} = \sqrt{v_{J_-}^2 + v_{J_+}^2 + v_{IN_-}^2 + v_{IN_+}^2} = 159\mu V$$

next to the 164μV measured.

Figures from 4.18 to 4.23 show noise level and spectrum for each channel. Figures 4.24 and 4.25 show buffered and amplified channels' spectrum density.

Note: for the measure showed in Fig. 4.25 was used a front-end board with a 5x gain instead of 10x. To relate the obtained value to a 10x channel it must be multiplied for a 2 factor.

4.4 LVDS output: discriminator activation and jitter

In Fig. 4.26 is showed the discriminator activation sending the LVDS differential output to the oscilloscope through a differential probe.

For the jitter measurement on the LVDS output was used a LeCroy Wavepro 735Zi, 3.5GHz, 20GS/sec *digital oscilloscope*. *Jitter* is the deviation from true periodicity of a presumed periodic signal, often in relation to a reference clock source - the LeCroy has a really high clock accuracy (< 1ppm).

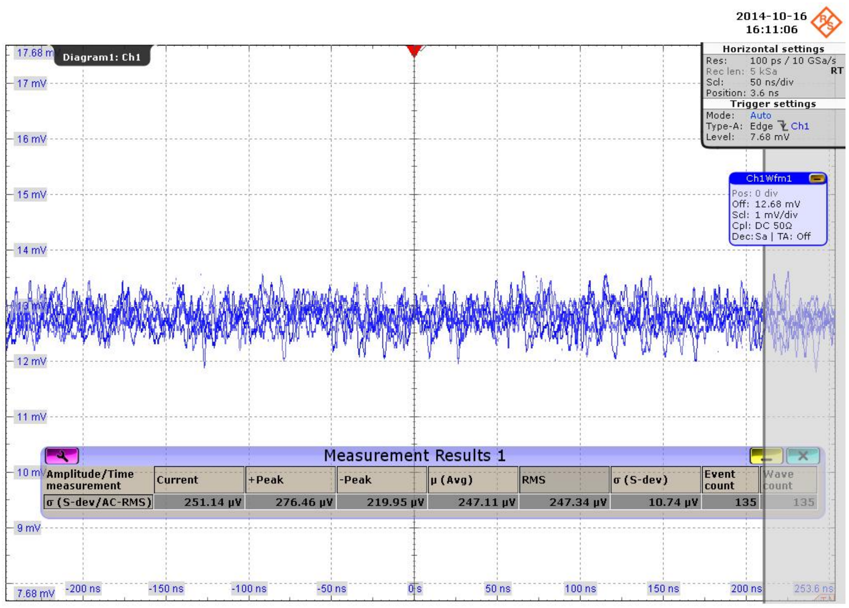


Figure 4.18: Noise level of the fast channel.

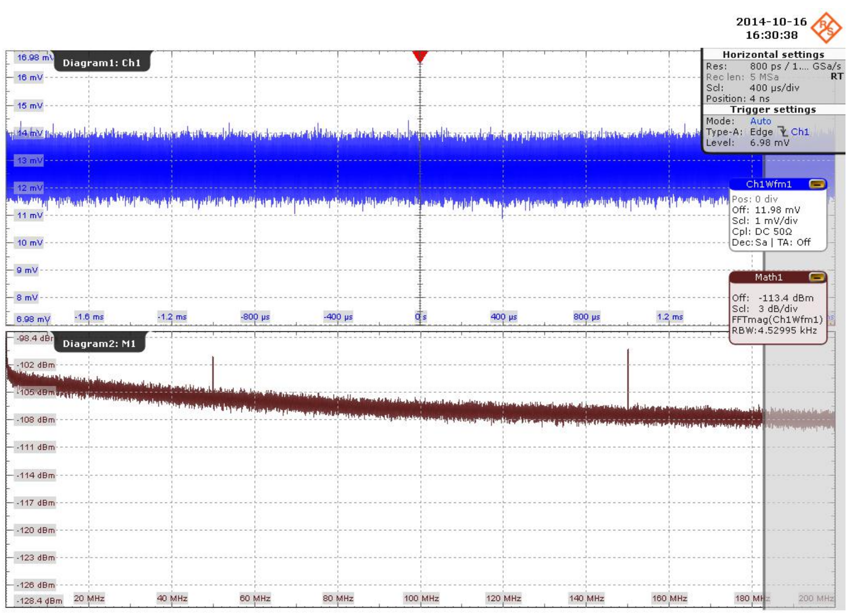


Figure 4.19: Noise spectrum of the fast channel.

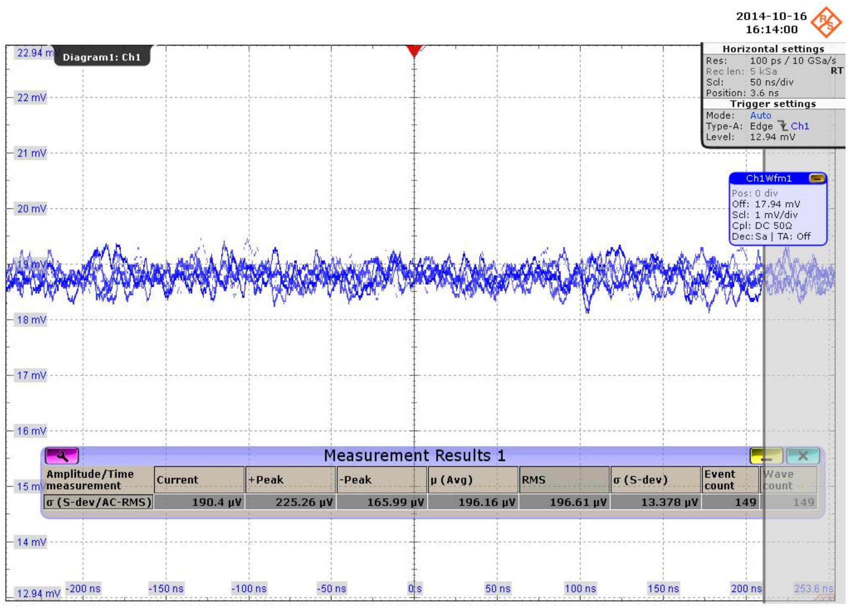


Figure 4.20: Noise level of the filtered channel.

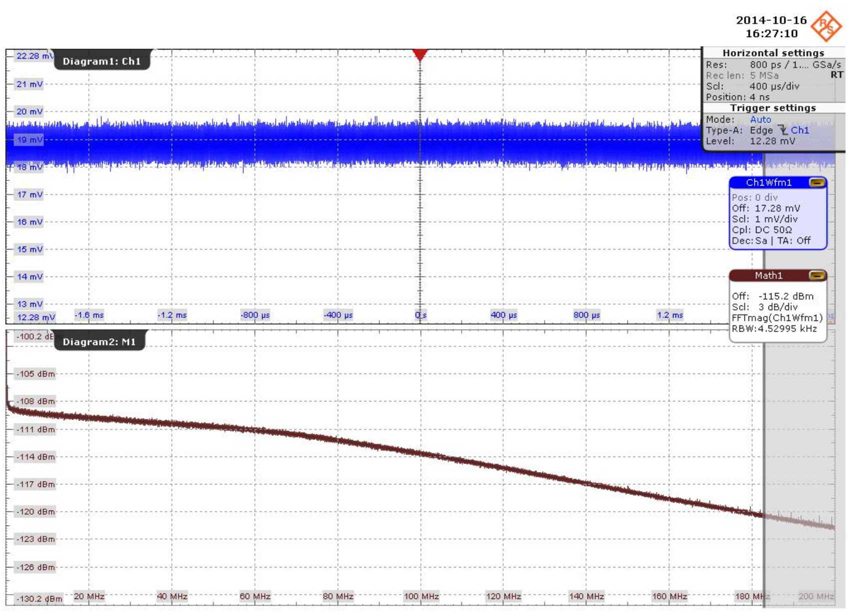


Figure 4.21: Noise spectrum of the filtered channel.

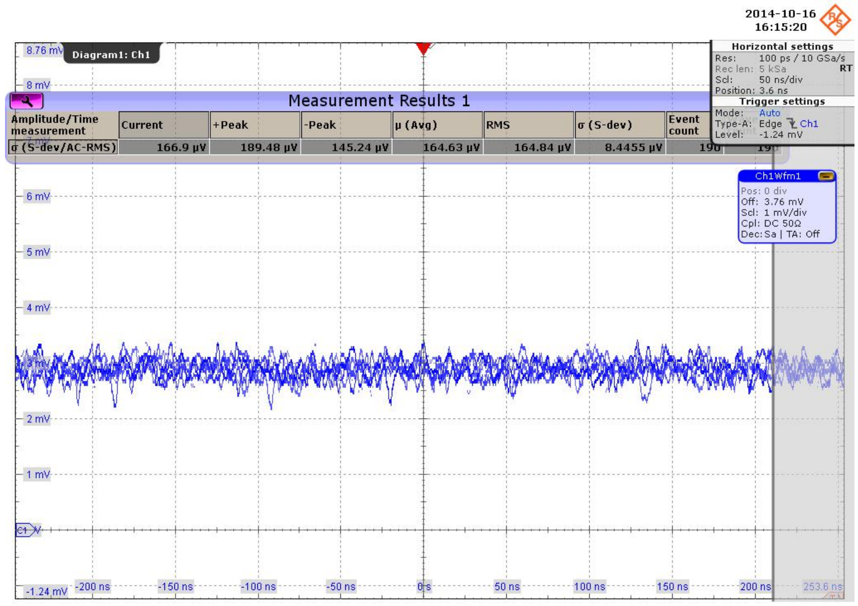


Figure 4.22: Noise level of the buffered channel.

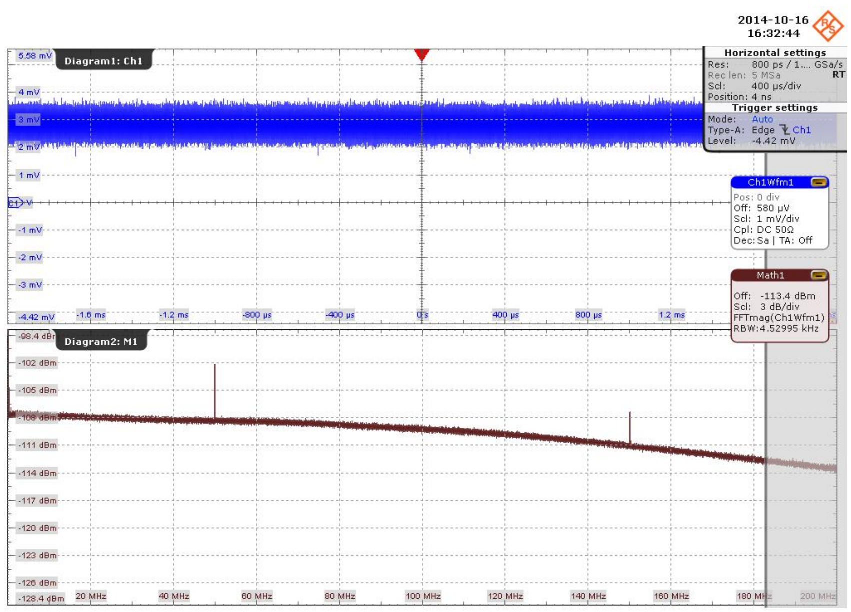


Figure 4.23: Noise spectrum of the buffered channel.

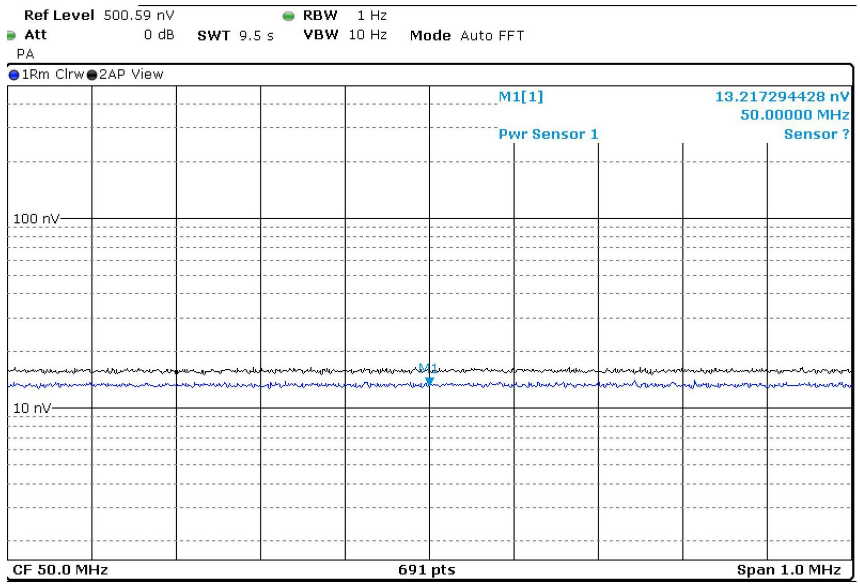


Figure 4.24: Noise spectrum density of the buffered channel.

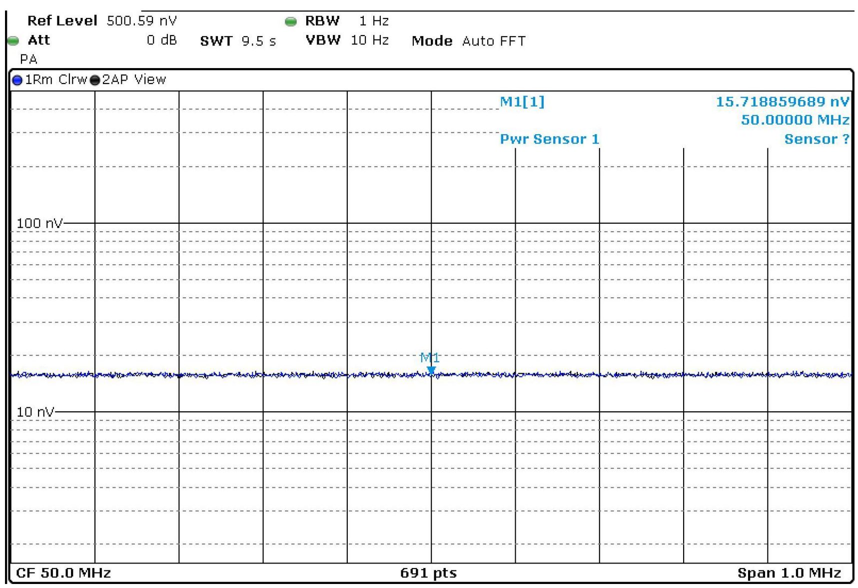


Figure 4.25: Noise spectrum density of the buffered channel.

Figure 4.26: Discriminator activation: the LVDS output.

Jitter may be observed in the frequency of successive pulses. It can be *deterministic* or *random*: the first is predictable and reproducible, the second is unpredictable and can be considered a consequence of thermal noise (see Appendix A). It is quantified using the standard deviation of a Gaussian distribution: the LeCroy can calculate it, as showed in Fig.4.27, with the result of a jitter of 18ps.

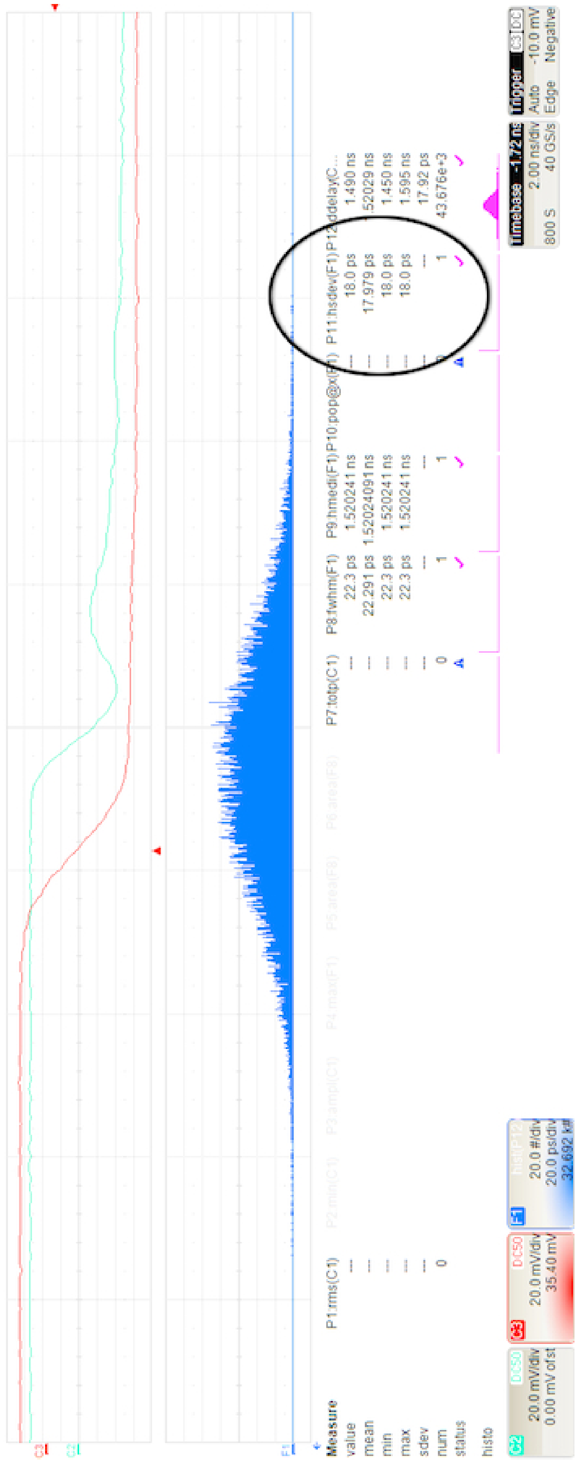


Figure 4.27: Jitter standard deviation.

Chapter 5

Summarizing

This board is greatly designed. The main purpose of keeping an ultra-low noise level is reached, sometimes so perfectly that the behavior of the system is practically a confirm of the components' characteristics as indicated by manufacturers in datasheets.

The following table summarizes the obtained results.

Channel	**Gain**	**Bandwidth (MHz)**	**Fall Time (ns)**	**Noise (μV)**
Fast	10	282	1.61	247
Filtered	10	97	3.37	196
Buffered	1	50	7.29	164

For the LVDS output, the jitter is 18ps.

Appendix A

Noise

In electronics can not exist a signal totally clean: it will always have a certain amount of *noise* overlapped on itself that could considerably affect the circuit expected functioning. A generic signal $v(t)$ will therefore be expressed through:

$$v(t) = s(t) + n(t) \tag{A.1}$$

where $s(t)$ is the ideal clean signal and $n(t)$ the noise signal overlapped. For its nature, noise is a *random signal*: it will be different at any instant of time. Therefore $n(t)$ has an unpredictable shape in time, making it a useless characterization to study its effects. The best way to examine noise is to make a probabilistic analysis of its values to obtain its statistical distribution. The two fundamental parameters to calculate are:

- the average value of the measures,

$$\bar{x} = \frac{\sum_{i=0}^{N} x_i}{N} \tag{A.2}$$

- the *standard variation*,

$$\sigma = \sqrt{\frac{\sum_{i=0}^{N} (x_i - \bar{x})^2}{N}} = \sqrt{\overline{n^2(t)}} \tag{A.3}$$

In particular, most of the times the noise follows a Gaussian distribution and presents a null average value. In this case, the standard variation characterizes the entity of the fluctuations of the noise. It is commonly indicated as Root Mean Square value, or RMS value.

The quantity $\overline{n^2(t)}$ is the noise power, usually called Mean Square value. It can be calculated in a different way than above, with an approach in the frequency domain. As any electric signal, noise can be expressed as the sum of sine waves thanks to Fourier's work. In example, *white noise* is a kind of noise signal with constant power at all frequencies. To extract the generic sine wave at the f frequency, we can think about filtering it with a band-pass filter centered on f and having a Δf bandwidth (this is what a spectrum analyzer does). It will output only the sine waves with frequency between $f - \frac{\Delta f}{2}$ and $f + \frac{\Delta f}{2}$, that we will indicate as $n_f(t)$. Each wave's temporal shape will be random, because the noise itself is a random signal; therefore, it will be characterized by $\overline{n_f^2(t)}$. We can now define a parameter which allow to calculate the power of the whole package of waves allowed to pass through the filter, called *power spectral density* $S(f)$:

$$S(f) = \frac{\overline{n_f^2(t)}}{\Delta f} \tag{A.4}$$

measured in $[V^2/Hz]$. Varying the central frequency of the filter we can measure the power spectral density for each frequency that composes the noise, obtaining its *power spectrum*. The whole noise power can then be calculated as follows:

$$\overline{n^2(t)} = \int_0^\infty S(f)df \tag{A.5}$$

It is important to specify that if the noise bandwidth is reduced(and this can be easily realized with filters), noise power will be lowered as well. This is a common practice in circuit design, and in this work there are a few examples on how it is done.

Johnson-Nyquist thermal noise

The electronic noise generated by the *thermal agitation* of the charge carriers (usually the electrons) inside an electrical conductor at equilibrium, which happens regardless of any applied voltage, is called *Johnson-Nyquist noise* (from the name of the ones who measured and explained the phenomenon) or simply *thermal noise*.

Thermal noise in an ideal resistor R is approximately white. The power spectral density, mean square value per hertz of bandwidth, is given by:

$$\overline{v_n^2} = 4K_B T R \tag{A.6}$$

where $K_B \simeq 1.38 \cdot 10^{-23}$J/K is Boltzmann's constant, T is the resistor's absolute temperature in K, and R is the resistor value in Ω. For a given bandwidth, the root mean square (RMS) of the voltage, v_n, is given by:

$$v_n = \sqrt{\overline{v_n^2}} \cdot \sqrt{\Delta f} = \sqrt{4K_B T R \Delta f} \tag{A.7}$$

and the related power if the resistor in short circuit is

$$P = \frac{v_n^2}{R} = 4K_B T \Delta f \tag{A.8}$$

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